A comprehensive fault diagnosis technique for reversible logic circuits ☆

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ABSTRACT

Fault diagnosis is a complex and challenging problem in reversible logic circuits. The paper proposes a novel fault diagnosis technique for missing control faults in reversible logic circuits. The main focus of this technique is to extract the unique fault signature for each missing control fault in the circuit. The fault signatures are the sequences of test vectors to identify the location of the faults. Based on these fault signatures a unique fault diagnosis tree is built. Our proposed fault diagnosis algorithm is used to traverse the fault diagnosis tree to find the presence and location of the fault. The traversal process is simple and fast. The algorithm executes in linear time and experimental results for benchmark circuits show the reduction of test patterns compared to earlier works.

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1. Introduction

Energy consumption has become a critical issue in digital circuit design. In any logic computation, a certain amount of energy is dissipated for every bit of information-lost regardless of the technology adopted for implementation [1]. Reversible computing performs lossless information processing and theoretically provides zero power dissipation. Recently it has come out as a flourishing research topic. Reversible circuits that carry reversible computations are considered as a special class of quantum circuits. Quantum computations are exponentially faster than classical computations. It can perform huge parallel computations in a single step and solve many problems such as prime factorization much more rapidly than that of non-quantum approaches [2,3]. Quantum circuits have applications in the field of low power circuit design, nanotechnology, bioinformatics, cryptography and many others.

In quantum computing the information is stored in the form of qubit (q-bit) instead of bits that are used in classical circuits (non-quantum). Qubits are microscopic entities such as a photon or atomic spin. A qubit can be in a zero or a one state, conventionally denoted by |0> and |1> respectively. However, it can also be in a superposition of these states, i.e., $\alpha_0|0> + \alpha_1|1>$, where α_0 and α_1 are complex numbers called amplitude [4–6].

Automated synthesis and testing of reversible circuits have attracted as a major research challenge. Fault models and testing approaches [7–9] are proposed by researchers in recent years. Automatic Test Pattern Generation is an electronic design

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automation method used to find an input (or test) sequence that distinguishes between the correct circuit behavior and the faulty circuit behavior caused by defects. ATPG based techniques for reversible circuits are introduced by Wille et al. [10]. But to the best of our knowledge very few works are published in the area of fault diagnosis in reversible circuits so far. The aim of fault diagnosis is to find out the location of faults. To perform an efficient diagnosis, a test set with good diagnostic capability is needed. Therefore, diagnostic ATPG is a critical part of fault diagnosis. In diagnostic test generation, the goal is to find a test sequence such that the circuit produces a different response for different faults present in the circuit. The problem of diagnostic test generation is much harder than conventional test generation, since it has to deal with pairs of faults.

Fault localization in reversible circuits by using adaptive tree is introduced by Ramasamy et al. [11]. Another approach generates fault localization tree to locate the fault. Both the techniques consider all possible input assignments to identify the faulty behavior of the circuit. Error debugging has been introduced in [12,13]. Fault masking using majority voters with error masking capabilities for reversible circuits is presented in [14]. Pierce et al. [15] presents the test set generation and fault localization software for reversible circuits. Fault diagnosis in reversible circuits under missing-gate fault model is proposed in [16]. A new fault diagnosis technique [17] is proposed that explicitly exploits the advantageous properties of reversible circuits.

In this paper, we address the problem of the fault diagnosis under missing control fault model in reversible logic circuits. The proposed fault diagnosis technique is used to locate the presence of faults and to find the presence of equivalent faults in the circuit. Pseudorandom test vectors are applied to the circuit and from the output responses of the faulty and the fault free circuit a fault analysis table is constructed. Unique signatures for each of the missing control fault are found and stored in the fault diagnosis table. Next, the fault diagnosis tree is built from the fault signatures. Fault diagnosis is performed by traversing this tree. The proposed method rapidly identifies the presence of any missing control fault in the circuit.

The structure of rest of the paper is as follows: a brief idea of reversible logic circuits and reversible logic gates and their basic properties are discussed and the model of missing control faults is introduced in Section 2. The proposed fault diagnosis technique with illustration is presented in Section 3. Experimental results are shown and conclusions are drawn in Sections 4 and 5 respectively.

2. Preliminaries

In this section the basic properties of reversible circuits and reversible logic gates are presented. We have also discussed about the fault model that is used in our proposed work.

2.1. Reversible logic circuit

A circuit is said to be reversible if the (Boolean) function it computes is bijective i.e., there is one-to-one and onto correspondence between its inputs and outputs. The input vector can be uniquely determined from the output vector and vice versa. A necessary condition is that the circuit has the same number of input and output wires. No fanout is allowed and it is a loop free circuit. A block diagram of an n-input n-output ($n \times n$) reversible circuit is shown in Fig. 1.

An $n \times n$ reversible logic circuit $G = g_1, g_2, g_3, \ldots, g_d$ is a cascade of d reversible logic gates. The block diagram of a reversible circuit that is a cascade of d reversible gates is shown in Fig. 2. Most of the classical gates like AND, OR, XOR are not reversible. Controlled-NOT (CNOT) gate proposed by Feynman, Toffoli gate, and Fredkin gate are well known reversible logic gates.

Fig. 3 shows a 3×3 reversible circuit of 6 reversible logic gates. It computes the bijective function (0, 1, 2, 3, 4, 5, 6, 7) → (7, 0, 1, 3, 4, 2, 6, 5). The input output mapping by a truth table is shown in Table 1.

2.1.1. Representation of reversible circuits by unitary matrix

A unitary matrix U of order n is an $n \times n$ matrix whose entries are complex number and whose inverse is equal to its conjugate transpose $\overline{U}$. This means that $\overline{U}U = U\overline{U} = I$, where $\overline{U}$ is the conjugate-transpose of U and I is the identity matrix. The elements of a unitary matrix satisfy the relations

$$u_{i1}\bar{u}_{k1} + u_{i1}\bar{u}_{k2} + u_{in}\bar{u}_{kn} = \begin{cases} 1 & if \ i = k \\ 0 & if \ i \neq k \end{cases}$$
$$(i, k = 1, 2, \ldots, n)$$

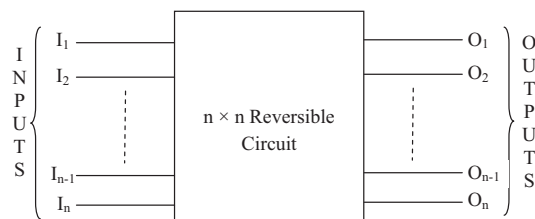**Fig. 1.** Block diagram of an n-input n-output reversible circuit.