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# Power-aware system-on-chip test scheduling using enhanced rectangle packing algorithm ☆

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ABSTRACT

The current semiconductor technology allows integration of all components onto a single chip called system-on-chip (SoC), which scales down the size of product and improves the performance. When a system becomes more complicated, testing process, such as test scheduling, becomes more challenging. Recently, peak power has also been considered as constraints in the test scheduling problem. Besides these constraints, some add-on techniques including pre-emption and non-consecutive test bus assignment have been introduced. The main contribution of each technique is the reduction of idling time in the test scheduling and thus reducing the total test time. This paper proposes a power-aware test scheduling called enhanced rectangle packing (ERP). In this technique, we formulate the test scheduling problem as the rectangle packing with horizontally and vertically split-able items (rectangles) which are smaller to fill up more compactly the test scheduling floor plan. Experimental results conducted on ITC'02 SoC benchmark circuits revealed positive improvement of the power-aware ERP algorithm in reducing total SoC test time.


## 1. Introduction

Spurred by the advancement of semiconductor technology that permits a system to be integrated on a single chip, the gap between design and manufacturing becomes larger. Besides the need of more powerful design tools to close the gap between the capability of engineering design and that of semiconductor technology, efficient test methodologies and high-performance automated test equipment (ATE) are essential. Required test time reduction is as much as 2.5 times in 2013, as predicted in Ref. [1]. Among the processes in VLSI testing, test development and design-for-testability involve the introduction of test architecture for system-on-chip (SoC) including test wrapper and test bus called test access mechanism (TAM), and scheduling of test data to SoC. Besides the optimal design of test wrapper and TAM, the test planning framework should be developed in such a way that test data for a SoC can be scheduled for minimum test time. In addition, power and thermal are becoming much more dominant factors for deep sub-micron technologies, and they should be considered in the test planning.

Basically, test scheduling is a process to determine when each test set is to be executed in order to minimize the test time. One of the earliest works that studied SoC test scheduling is done by Chakrabarty [2] at the beginning of the millennium. He solved the test scheduling problem using mixed integer linear programming (ILP). Then, Iyengar in his works [3,4] proposed

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that test scheduling can be formulated as rectangle a packing problem for SoC with basic test architecture, i.e. TAM and test wrapper with external test resource of ATE. The test architecture is based on IEEE Standard P1500 introduced in Refs. [5,6]. Earlier works had been solving the test wrapper design and TAM for test scheduling independently. It's not until 2002, when Iyengar et al. [3,4] introduced the approach to cater for test wrapper and TAM design optimization in-conjunction by proposing an integrated wrapper/TAM design co-optimization, which has effectively balanced out the wrapper scan chain length for test application time optimization in any given TAM width. Zou et al. [7] then further improved the test wrapper design by considering the core without internal scan chains. With the establishment of balanced wrapper scan chain concept for test wrapper and TAM design, more focus has been put on the optimization of SoC test scheduling algorithm and the co-optimization of wrapper design and test scheduling as shown in previous works of Refs. [8,9].

Some other techniques were considered to further reduce the total test time. They are pre-emption and non-consecutive TAM assignment. In addition, test scheduling technique is developed such that it is applicable to SoC with multiple clock domain [10,11], hierarchical cores [12] and combination of external and internal test resources [13]. Xia et al. [14] proposed an enhanced test scheduling technique whereby test time was further reduced through non-consecutive TAM assignment, which is viewed as a vertical rectangle splitting in the rectangle packing algorithm. Smaller rectangles produced by this vertical splitting are able to fill up the idling time resulted from method [4] and thus reducing the SoC total test time. However, due to the restriction of only vertical splitting being allowed, there is still room of improvement. Rectangle packing algorithm with vertical splitting has inspired the following research works that produce a more optimized test scheduling algorithm. Random insertion (RAIN) scheduling algorithm introduced by Im et al. [15] achieved its optimization by random position insertion onto the sequence pair representation of rectangle placement. Ahn and Kang engaged ant colony optimization (ACO) approach [16] to tackle the test scheduling problem that was formulated as a rectangle bin-packing problem. However, little improvement was obtained compared to Ref. [15]. Yu et al. [17] proposed a two-stage genetic algorithm (GA) to solve the test scheduling problem that has been formulated into a 2-dimension floor-plan problem with sequence pair architecture. It shows shorter test time for two of the ITC'02 SoC benchmark circuits compared to Refs. [2] and [7]. Another genetic algorithm (GA) model for optimal test scheduling was then proposed in Ref. [18] where the differential evolution and self-adaptive mutation were brought into the traditional genetic algorithm. However, no experiment is conducted on ITC'02 benchmark circuits.

Iyengar and Chakrabarty [19] worked on further reduction of test time through pre-emption technique. Pre-emptive test scheduling means that testing of a core can be stopped and resumed within the duration of testing. In other words, the testing can be divided into several parts. We call pre-emption as horizontal rectangle splitting in the test scheduling floor-plan. Nevertheless, [19] did not explain whether the second part of testing could be done using different portions of test bus or not upon the resumption. On one hand, minimizing test time requires as many cores as possible are tested concurrently [2–4,7–9]. On the other hand, concurrent testing results in higher power dissipation. Thus, power issues are needed to be taken into consideration, similar to hotspots, which must be taken good care of to avoid chip damage due to high temperature. Therefore, test scheduling problem should be solved so that total test time of a SoC is minimized under power constraint.

Recently, system-level peak power has been considered as a constraint in test scheduling problem. If these are not considered, power may exceed the limit, which can damage the chips under test. Huang et al. [20] extended the rectangle representation concept into a 3-dimensional bin-packing problem to include power constraint on the third axis and proposed a best-fit heuristic method to solve the problem. Refs. [13,21] introduced a new integrated framework that allowed test planning with power consideration and proposed that test planning could be done at the earlier stage of SoC design. While Wuu et al. [22] applied the B*-tree based floor-planning technique to address the similar issue, Harmanani and Farah [23] proposed an optimization method based on simulated annealing, which can handle precedence constraints that preserve the desirable test ordering for SoC test scheduling with or without power constraints. Both Refs. [24] and [25] are taking design hierarchy constraints into consideration for SoC test scheduling optimization where Ref. [24] is based on simulated annealing technique and Ref. [25] is engaging genetic algorithm approach. In addition, Yoneda et al. [26] and Zhao [27] further consider the power-aware test scheduling for SoC with multiple clock domains.

Motivated by an improved memory allocation method introduced in Ref. [28] where the memory allocation problem is modelled by the bin-packing algorithm with split-able items, we propose a new test scheduling algorithm based on rectangle packing (RP) called *enhanced rectangle packing* (ERP). ERP splits the rectangles either horizontally or vertically when necessary in order to pack them more compactly in the given bin. Hence, the total test time can be further reduced. The remaining of this paper is organized as follows. In Section 2, we describe the terminology to be used and the SoC test scheduling problem. The proposed ERP algorithm is presented in Section 3. Power-aware heuristic is explained in Section 4. Section 5 shows the experimental result conducted on ITC'02 SoC benchmark circuits together with the result comparison between our proposed ERP algorithm and RP algorithm [4] with power constraint taken into consideration. Section 6 concludes the paper.

## 2. Preliminaries

Test wrapper is an interface between a core in the SoC and the test access mechanism (TAM) while TAM is a test bus that transports test data between SoC pins and test wrapper. Fig. 1 shows a TAM and a test wrapper that surrounds a core.

Test scheduling problem that is addressed in this paper is formally defined as follows.