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Novel low-cost and fault-tolerant reversible logic adders

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ABSTRACT

In recent years, reversible logic circuits have received considerable attention due to their diverse applications in various fields. As the computing systems are susceptible to different environmental effects which can impact their intended operations, having the fault-tolerance capability is of great importance. In this paper, at first, a novel reversible gate is presented to achieve a parity preserving full adder which serves as the main building block of different adders. Further on, by using the proposed full adder and new arrangements of other reversible gates, some new low-cost fault-tolerant adders including binary coded decimal, carry skip and carry look-ahead architectures are presented. The new adders are highly efficient in the quantum cost, total logical calculation and transistor count compared to the existing designs. In addition, regarding other factors including the number of gates, garbage outputs and maximum delay, they are the best or among the favorite parity preserving reversible adders.

1. Introduction

The processing elements based on the classical integration circuit designs will no doubt reach their physical limitations. However, before that, the high power dissipation in the VLSI circuits that are made according to the latest nanometer technologies has slowed down the scaling of these circuits based on the Moore's law. Therefore, many researchers are investigating the new design paradigms such as reversible computing to overcome the current major challenges. In fact, the ordinary or irreversible computations always lead to energy dissipations. R. Landauer in 1961 [1] was the first to demonstrate that losing one information bit leads to an energy dissipation of $kTLn2$ jouls in which k is Boltzmann's constant and T is the absolute temperature at which the computation is performed. In fact, some information is lost if it would not be possible to retrieve the input data from the output which is common in ordinary computations. After that, C. H. Bennett in 1973 [2] showed that no energy will be dissipated if a circuit only consists of reversible gates. Thus, reversible computing can be attractive to conquer one of the main challenges in computing systems by obtaining lower power circuits.

As a result of the inherent reversibility of closed quantum mechanical systems, quantum circuits are also reversible by their nature [3]. Therefore, reversible logic circuits can be used to build quantum computers in nano scales in order to benefit from both the reduction in energy dissipation and to reach a higher computational speed. As in the reversible circuits no information is lost and the input vector can be recovered from the output vector, there should be a one to one correspondence between the input and output vectors which means that the number of inputs should be equal to the number of outputs. However, if a fault occurs inside a reversible circuit, the output vector will be incorrect and as a result the input vector cannot be retrieved. Thus, the fault-tolerance capability is vital for reversible circuits due to the fact that

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these circuits, especially reversible low-power CMOS designs, are vulnerable to the environmental effects. A straightforward and low-cost method to achieve fault-tolerance is the use of the parity codes to detect errors in the output. This way, the parity preserving characteristic can be applied to reversible gates and circuits with a reasonable cost. In a parity preserving reversible gate, the parity of the input vector is equal to the parity of the output vector. However, as the feedback and fan-out are not permitted in reversible circuits [4], the synthesis of these circuits, especially fault-tolerant designs, is different and more difficult than the irreversible circuits.

So far, many reversible arithmetic operators have been designed to perform addition [5–12] and multiplication [3,13–17] that some of them are parity preserving and thus beneficial for fault-tolerant reversible circuits. In addition, some designs include proposing new gates and then utilizing them in the proposed adder or multiplier circuit such as [9,10,12,13], and the others are based on exploiting the new arrangements of the existing gates. In this paper, we employ both types of reversible circuit designs to attain the intended fault-tolerant reversible adder architectures. First, we propose a new low-cost reversible gate that after adjustment of its inputs, it operates as a parity preserving full adder. This full adder requires the minimum hardware complexity or the number of logical operations to prepare the output amongst the existing parity preserving full adders. Thereafter, by incorporating the proposed full adder and the innovative organizations of other required reversible gates, some adder architectures with the aim of being low-cost and parity preserving are proposed including ripple carry adder (RCA), binary coded decimal (BCD) adder, carry skip (CSK) adder and carry look-ahead adder (CLA). In addition, we will introduce a more precise delay computation not presented before to be used in the evaluation process of the proposed designs compared to their counterparts.

The rest of the paper is organized as follows. In Section 2 some preliminaries and the basic concepts mainly regarding the reversible gates are described. In Section 3 the related works, and in Section 4, the proposed reversible gate needed for designing the low-cost parity preserving full adder is explained. The new low-cost fault-tolerant reversible adder architectures are described in Section 5. Section 6 presents an approach for the transistor realization of the proposed gate and adder architectures. Section 7 illustrates a new delay estimation approach. The evaluation of the proposed reversible adders compared to the existing designs are presented and discussed in Section 8. Finally, some conclusions and future works are drawn in Section 9.

2. Preliminaries

2.1. Basic concepts

A logic gate is reversible if there is a one to one correspondence between its input vector and output vector. Each output vector is uniquely determined from the input vector, and each input vector is uniquely recovered from the output vector. A reversible gate is denoted by $n \times n$ which means that the number of inputs is n and equals the number of outputs. A circuit is reversible if it only consists of reversible gates.

In a reversible gate or circuit the garbage outputs are the outputs that would not be used in the subsequent computations. In other words, the outputs that are solely needed to maintain reversibility are called garbage outputs [7]. In addition, the constant inputs are the inputs whose values do not change in a gate and have to be maintained at either 0 or 1 in order for the gate to perform the intended function. These inputs are also added to a gate to make it reversible [18].

The quantum cost is defined as the number of 2×2 quantum primitives required to implement a reversible gate. All quantum primitives of the form 2×2 have a unit quantum cost such as CNOT (controlled NOT), V and V^+ in which V is the square-root of NOT gate and V^+ is its Hermitian. Thus, $V \times V = V^+ \times V^+ = \text{NOT}$ and $V \times V^+ = V^+ \times V = I$ that is an identity matrix. In addition, the NOT gate is a 1×1 quantum primitive that has no quantum cost [7]. The reversible gates bigger than 2×2 gates cannot be directly realized by quantum techniques. Therefore, the quantum primitives should be used for implementation of the bigger gates. Another criterion in the design of reversible circuits is the total logical calculation that includes the number of XOR, AND, and NOT operations appeared in the output expressions. Therefore, the hardware complexity is proportional to the number of logical operations required to prepare the outputs. In other words, it reflects the computational complexity of a reversible circuit. Another important criterion is the delay of a reversible circuit that is defined as the maximum number of gates on the paths from the inputs to the outputs [7].

So far many reversible gates are designed. However, some of them as the basic gates are more frequently used in the reversible circuits. In the following, these gates are introduced in two classes.

2.2. Simple reversible gates

The most important simple gates are Feynman gate (FG) [19], Toffoli gate (TG) [20] and Peres gate (PG) [21]. The block diagram and quantum realization of FG which is also called CNOT are represented in Fig. 1. In addition, Table 1 shows its truth table. Based on the function of FG and its truth table, its reversibility is evident. This 2×2 gate can also be used as the equivalent of fan-out operation in reversible circuits when its B input is set to zero. The block diagram and quantum realization of TG are shown in Fig. 2 as a 3×3 reversible gate. This gate can be considered as a universal reversible gate that means any reversible logic circuit can be implemented only by using this gate after the proper setting of some inputs to one or zero to produce the Boolean functions. The block diagram of PG is shown in Fig. 3 as the lowest-cost universal