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A hybrid packet-circuit switched router for optical network on chip ☆

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ABSTRACT

The increasing number of Intellectual Property (IP) cores challenges the traditional electrical Network on Chip (NoC). Silicon nanophotonics becomes a leading technology because of offering several benefits for NoC. Also, On-chip services, including guaranteed service and best-effort service, have different traffic characteristics. This has an important influence on the performance of NoC. This paper proposes a hybrid packet-circuit switched router for optical Network on Chip (ONoC). It can support optical circuit switching (OCS) and optical packet switching (OPS) in parallel and simultaneously, in order to optimize the performance of the network with both services. According to the simulation results, the proposed architecture achieves lower latency and higher throughput than the traditional architectures in the same network scale.

1. Introduction

With the integration density increment of a single chip, the recent development in the chip design indicates a progress towards the multi-core era. As the number of Intellectual Property (IP) cores integrated in a single chip increases, the performance of the Network on Chip (NoC) is being limited in aspects of power consumption, data latency, throughput, and so on. The global interconnect becomes a critical determinant of the entire network performance, because it plays an important role in the interconnection of IP cores. There is an increasing need for the traditional electrical interconnect to meet the speed and highly-scalable throughput in the network with large numbers of IP cores. However, the electrical interconnect performs not so well in the areas of power efficiency and performance scalability [1]. Also, there is a reliability problem [2].

One solution to solve these aforementioned bottlenecks is the optical interconnect, with higher speed of signal propagation, higher bandwidth density and lower power dissipation. Based on the Silicon-on-Insulator (SOI) platform, many optical devices that can be applied in NoCs have significant advances [3–9]. This makes the optical interconnect an attractive technology. As a result, based on silicon photonics, several architectural designs for NoCs have been proposed by various research groups.

The services in NoCs can be roughly classified into two categories: the guaranteed service and the best-effort service. The traffic of different services has different characteristics separately. The guaranteed service needs to reserve some resources to guarantee the throughput, and most traffic of the guaranteed service is longer in the length and more continuous in the time. The best-effort service does not require the reservation of resources to guarantee the performance, and the traffic of the best-effort service is generally short in the length and burst in the time. The design of the router architecture is mainly dependent on the traffic characteristics in the chip. Thus, a router that can satisfy the requirements of two categories of traffic at the

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same time would present some advantages in terms of delay, throughput and cost. Most of the current designs utilize only one kind of switching mechanisms, optical circuit switching (OCS) or optical packet switching (OPS). However, if the traffic of different services is handled with the same switching scheme, the network efficiency may be low and the communication cost can be high.

In the optical Network on Chip (ONoC), OCS can process the traffic of the guaranteed service effectively, but it is not so effective for the best-effort service [10]. OPS is more efficient for the traffic of the best-effort service, but it is inefficient for the guaranteed service. To meet the traffic requirements of the guaranteed service and best-effort service simultaneously, we present a hybrid switched router for ONoC. The proposed router processes the traffic of different services separately, by separating the traffic in different wavelengths. Thus, it can support OCS and OPS mechanisms in parallel.

The rest of the paper is organized as follows. Section 2 gives a brief introduction of the current related works in ONoCs. Section 3 gives a detailed description of the proposed router, including the architecture, the schemes of switching, the flow control, and the contention resolution. In Section 4, we analyze the performance of optical power and loss, and evaluate the network performance with simulations. Also, a performance comparison of different architectures is made. Finally, conclusions are presented in Section 5.

2. Related works

The optical interconnect exhibits better performance than the electrical alternative. Several ONoC architectures composed of nanophotonic devices have been proposed. Cianchetti et al. [11] propose a hybrid electrical/optical network called Phastlane. The router of the network can optically transmit packets several hops in the network, with electrical buffers to solve the blocking problem. Joshi et al. [12] propose a network named as Clos. It uses the silicon-photonic technology for the global on-chip communication. This exploits multiple stages of small routers to form a larger non-blocking network. Pan et al. [13] present a hierarchical topology based on clusters, Firefly. In this network, the electrical interconnect is used for the local intra-cluster communication and the optical crossbars for the global inter-cluster communication. The global crossbar is implemented by the bus waveguides. Shacham et al. [14] propose a 2D photonic NoC architecture, consisting of an electrical network and a photonic network. The control information is handled in the electrical network, whereas the data transfer occurs in the photonic network. Before the data transmission being processed, an electrical path setup packet is routed in the electrical network to reserve the resources of the optical network from the source to the destination. This is for establishing an optical data path. After the success of the path establishment, the data transfer begins. In the end, a packet is sent to tear down the established path. Corona, a 3D many-core optical architecture targeted for a 16 nm process in 2017, is developed by Vantrease et al. [15], with a photonic crossbar interconnecting 256 cores in 64 four-core clusters. The crossbar is realized by numerous many-writer single-reader buses, combining with wave-division-multiplexing (WDM) to provide higher bandwidth. To resolve the conflict, a token-based arbitration scheme is used to allocate the available channels to clusters. Kirman et al. [16] present a hierarchical opto-electrical system based on the shared ring-bus to support the snoopy cache coherence in future Chip Multiprocessors (CMPs). The total 64 cores are organized in four nodes, each with four cores and a shared L2 cache communicating electrically. The bus architecture is employed for the inter-node communication. Batten et al. [17] develop a new processor-memory network in mesh topology based on an opto-electrical global crossbar, in order to provide the performance improvement in the manycore bandwidth. Miller et al. [18] present a tiled multicore architecture based on snake-shape waveguides, aiming at the technology node of 11 nm in 2019 with at least 1000 cores. Two networks exist, the electrical network for the short-range communication and the optical network for the global communication. Kirman and Martînez [19] propose a design for ONoCs, composed of passive optical wavelength routers. The routers are incorporated with the wavelength-based routing algorithm and oblivious routing algorithm to construct an all-optical network for CMPs. Koohi et al. [20] present an all-optical NoC in a new proposed regular and scalable topology, named as 2D-HERT. It employs a new kind of optical switch called WaROS. Li et al. [21] introduce an optical on-chip network, including a broadcast/multicast subnetwork for the latency-critical communication traffic and a circuit-switching subnetwork for the throughput-critical communication traffic. This optimizes the performance of the latency and throughput. Brière et al. [22] study an ONoC based on the λ-router. The switching is completed depending on the wavelength value of the optical signal. Pasricha et al. [23] propose an on-chip communication architecture based on an optical ring bus for the next generation Multi-Processor Systems-on-Chips (MPSoCs). The optical ring interconnects are used to replace the global pipeline electrical interconnects. This can overcome the bottleneck of electrical interconnects. Wu et al. [24] present a unified inter/intra-chip optical network, called UNION. It utilizes a hierarchical optical network to separate the inter-chip communication traffic from the intra-chip communication traffic. The local processor cluster is connected by electrical interconnects while the communication among the clusters is done by optical interconnects. A centralized control method is used to configure paths. This is a novel optical circuit switching method. Beux et al. [25] propose the Optical Ring Network-on-Chip (ORNoC) which is contention-free. Electrical interconnects are used in the intra-cluster/intra-layer, while optical interconnects are utilized in the inter-cluster/inter-layer. The same wavelength may be used in a single waveguide, providing wavelength sharing.

Compact optical routers are essential components for ONoCs. Biberman et al. [26] design a nonblocking four-port photonic router for ONoCs employing eight microring resonators. The switch-state of the microring resonator is configured by using direct-current resonance tuning. For different applications in the photonic NoC, Ji et al. [27,28] propose a four-port optical router and a five-port optical router, based on microring resonators. Both of the routers are non-blocking. The mic-