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Integrated core selection and mapping for mesh based Network-on-Chip design with irregular core sizes

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ABSTRACT

Network-on-Chip (NoC) has been proposed to replace traditional bus based System-on-Chip (SoC) architecture to address the global communication challenges in nanoscale technologies. A major challenge in NoC based system design is to select Intellectual Property (IP) cores for implementing tasks and associate the selected cores to the routers to optimize cost and performance. These are commonly known as the process of core selection and application mapping respectively. In this paper, integrated core selection and mapping problem has been addressed. Mesh architecture has been considered for experimentation. The integrated core selection and mapping problem takes as input the application task graph, topology graph and a core library. It outputs the selected cores for the tasks and their mapping onto the topology graph, such that, all communication requirements of the application are satisfied. The cores present in a core library may perform more than one task and have non-uniform sizes. For this, a technique based on Particle Swarm Optimization (PSO) has been proposed to select cores from the given core library and map the resultant core graph onto mesh based architectures. An efficient heuristic for mapping has also been proposed, which maps the selected cores onto mesh based architectures, considering non-uniform core sizes. Comparisons have been carried out with step-by-step core selection and mapping approach and also with mapping algorithms that exist in the literature. Significant reductions have been observed in terms of communication cost over all the cases. Area comparisons have also been made. On average, improvement of 13.05% in communication cost and 2.07% in area have been observed. The proposed approach has also been compared in dynamic environment and significant reductions in the average network latency could be observed. On average, improvement of 5.48% in average network latency and 15.68% in network throughput has been observed. Comparison of energy consumption has also been done in both the cases.

1. Introduction

Network-on-Chip (NoC) has emerged as a viable approach to implement Intellectual Property (IP) core-based designs, popularly known as System-on-Chip (SoC). It can handle efficiently the high bandwidth communication requirements between system components with the help of an underlying on-chip network consisting of routers and interconnects. The cores are attached to the local ports of routers, while the global router ports are interconnected between themselves in different topologies, such as, mesh, tree, etc [1,2]. Such system design methodology is largely dependent on the reuse policy and third-party cores. Preexisting modules are often integrated to achieve the desired functionality of the system. The cores integrated may be homogeneous in nature, each one being capable of implementing same set of tasks. This gives rise to the Multi-Processor System-on-Chip (MPSoC) architecture. The more general one is the heterogeneous structure in which each core used is capable of performing only a subset of tasks. The sizes of the cores may also vary.

The NoC design problem can be visualized as a sequence of steps as noted in Fig. 1. The input to the synthesis problem is the application task graph. The graph consists of nodes representing the tasks of the application. The tasks need to exchange messages between themselves, thus requiring varying communication bandwidths. The first step in the synthesis process is to select cores from a given core library. In a heterogeneous core library, each core is capable of performing a subset of application tasks. Assignment

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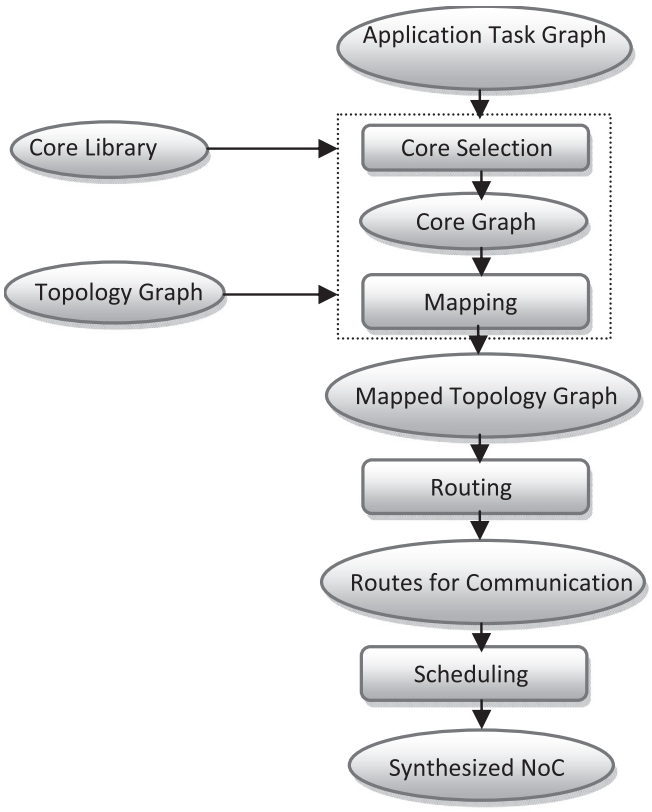

Fig. 1. Application-specific NoC design flow.

of tasks to cores gives rise to the core graph. Each node in the core graph corresponds to a selected core. One core may be assigned the job of realizing many task functionalities. Thus, the communication between task nodes in the application graph gets translated into bandwidth requirements of intercore communication.

The core graph is next mapped onto the specific topology graph. This stage is commonly known as Application Mapping. As will be noted in Section 2, many application mapping strategies have been reported in the literature. However, the first part, Core Selection, has not received that much attention. The core selection stage can significantly affect the mapping decisions as well. Since different selections of cores for the same application graph may lead to different core graphs, the mapping process will also result in different mapping solutions. Core size variations add another dimension to the NoC synthesis problem, as the mapping algorithm needs to take care of this aspect as well. Most of the mapping algorithms target mesh topology due to its regular structure with small interconnects. In this work also, it is proposed to target the mesh topology. However, there are very few works [33–37] that can handle non-uniform core sizes and irregular mesh structures. These techniques also lack in the core selection feature.

In this background, the present paper attempts to solve the integrated core selection and mapping problem. In the process, it also develops a new heuristic application mapping strategy for non-uniform core sizes, resulting in irregular mesh structure. To define the problem, a few definitions have been presented first.

Definition 1. *Application Task Graph (ATG)* is a directed weighted graph $A(T, E)$. Each node in T represents a task in the application. An edge corresponds to the communication requirement between the tasks. The weight of the edge represents the volume of communication. Each task $t_i \in T$ is of $type(t_i) \in F$, F being the set of all functionalities.

Definition 2. *Core Library* (L) is a library of IP cores. Each core c in it has associated dimension $dim(c)$ and can realize a subset f (subset of F) of functions. A task t can be realized by c only if $type(t) \in f$.

Definition 3. *Topology Graph* (TG) is an undirected graph $H(R, L)$ with the set of routers R, and a set of bidirectional links L between the routers. Each link has a capacity in terms of the maximum communication bandwidth that it can support.

A number of tasks in the ATG may get merged onto a single core. This creates the core graph for the application. Cores in the core graph are mapped onto routers in the topology graph. The cost of such a mapping is evaluated in terms of communication cost [27] which has direct correspondence with performance of the NoC and the network power consumption.

$$\text{Communication cost} = \Sigma\,(\text{No. of hops} * \text{Bandwidth between each pair of cores}, c_i, c_j \text{ in core graph}) \quad (1)$$

$(c_i, c_j) \in$ Edges of core graph

1.1. Problem definition

Given an application task graph A, a core library L and a topology graph H, select cores from L to realize tasks in A and map the resulting core graph onto H to minimize the communication cost, area, and power consumption of the NoC.

The salient contributions of the work are as follows.

1. Integrates core selection and mapping into a single problem. The core selection problem is an instance of set covering problem [3] whereas, the mapping problem is an instance of constrained quadratic assignment problem (QAP) [4], both of which are NP-hard. Hence formulation has been done based on a Particle Swarm Optimization (*PSO*) to solve the integrated problem.
2. Another major contribution of the work is the development of a heuristic application mapping procedure that takes care of non-uniform core sizes and can produce solutions in terms of irregular mesh architecture.
3. The heuristic mapping algorithm has been compared with well established techniques available in the literature.
4. Communication cost, floorplan area, throughput, latency and power consumption of the resulting networks for integrated and step-by-step solutions to the core selection and mapping problems, have been determined. It demonstrates the superiority of the integrated approach.

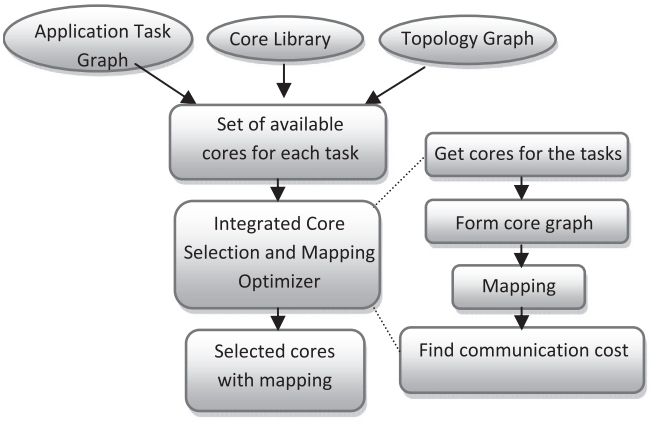

Fig. 2. Core selection phase in Application-specific NoC design flow.