Microprocessors and Microsystems 42 (2016) 10–23

Contents lists available at ScienceDirect

Microprocessors and Microsystems

journal homepage: www.elsevier.com/locate/micpro

Novel low power reversible binary incrementer design using quantum-dot cellular automata

Jadav Chandra Das[a], Debashis De[a,b,*]

[a] Department of Computer Science and Engineering, West Bengal University of Technology, BF-142, Salt Lake, Sector I, Kolkata 700064, India
[b] Department of Physics, University of Western Australia, Perth, Australia

ARTICLE INFO

Keywords:
QCA
Majority gate
Peres gate
Binary incrementer
Quantum cost
Reliability

ABSTRACT

This paper demonstrates the design of *n*-bit novel low power reversible binary incrementer in Quantum-Dot Cellular Automata (QCA). The comparison of quantum cost in quantum gate based approach and in QCA based design agreed the cost efficient implementation in QCA. The power dissipation by proposed circuit is estimated, which shows that the circuit dissipates very low heat energy suitable for reversible computing. All the circuits are evaluated in terms of logic gates, circuit density and latency that confirm the faster operating speed at nano scale. The reliability of the circuit under thermal randomness is explored which describes the efficiency of the circuit.

© 2015 Elsevier B.V. All rights reserved.

1. Introduction

In digital world, at hardware level, the most computational hurdle is the energy dissipation. Landauer [1] has proved that irreversible computation will have $k_BT\ln 2$ joules of dissipated energy due to loss of single bit information. This dissipated energy is considered as the lower bound to computation. Here, k_B and T holds for Boltzmann's constant and the computing temperature [2-3]. By resisting the loss of information bits, energy dissipation can be preserved. The most promising way out is reversible computation [3-4]. The computation in reversible circuit is carried out at logic level using bijective mapping, i.e., one-to-one mapping between input to output. Reversible circuits have no loss of information. The bijective mapping improves the observability and the controllability of the circuit [3-4]. It is expected that complementary metal-oxide-semiconductor (CMOS) technology will reach to its scaling limitation in next decade. Thus new nanotechnologies are being explored that has reduced dimensions and novel properties. As an alternative, quantum-dot cellular automata (QCA) technology has been proposed for CMOS technology. QCA is transistor-less technology, which combines the advantages of quantum dot and cellular automata logic together. QCA have several potential advantages like high density, fast operating speed, and very low power consumption [5-8]. In QCA, each bit of information is accumulated by using charge on electrons, present within QCA cell. Electrostatic interaction between QCA cells in a QCA circuit, caused transmission of bits through the circuit. Information processing technique used in QCA creates different and advance way to design logic circuit than that of CMOS circuit [9-12]. This paper deals with the reversible logic based design methodology of binary incrementer circuit and its implementation through QCA technology for the first time. The designs are achieved by employing Peres gate. The proposed QCA layouts and their simulation are executed through QCA Designer tool [13], which is a Bi-stable simulator engine.

Binary incrementer is essential to perform the increment operation on binary numbers in arithmetic logic unit. The irreversible nano-scale device originates high power dissipation. The solution is to employ reversible logic circuit, which has low power dissipation, i.e., ideally zero. Ultra low power dissipation of QCA device pledges the dominating implementation of reversible circuit at nano-scale than that of CMOS based design [2].

The contributions of this paper are as follows:

(1) QCA based design and implementation of Peres gate and reversible half-adder circuit.
(2) Design of *n*-bit reversible binary incrementer circuit using Peres gate.
(3) QCA implementation of proposed reversible incrementer circuit. The implementation is achieved for the first time.
(4) To achieve the QCA layout of half-adder and incrementer circuit, the same QCA circuit of Peres gate is employed.
(5) The estimation of quantum cost for both in quantum gate based technology as well as in QCA based technology is performed and also compared. The comparison shows the dominating design in QCA.
(6) Stuck-at-fault analysis for Peres gate is explored.

* Corresponding author. Tel.: +91 9830363215.
E-mail addresses: jadav2u@gmail.com (J.C. Das), dr.debashis.de@gmail.com (D. De).

http://dx.doi.org/10.1016/j.micpro.2015.12.004
0141-9331/© 2015 Elsevier B.V. All rights reserved.

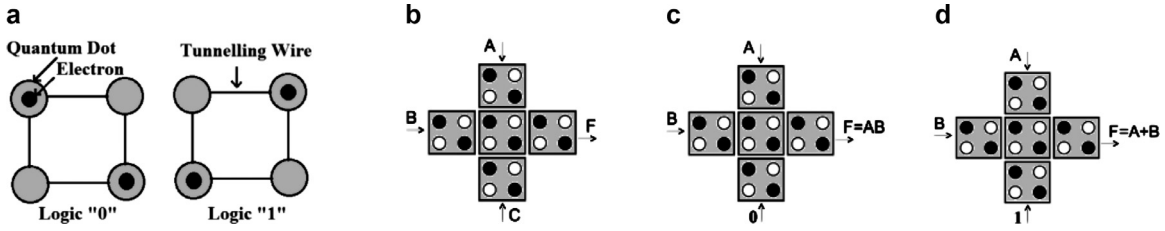

Fig. 1. (a) QCA cell with logic "0" as well as logic "1", (b) majority voter, (c) majority voter performing as AND function and OR function.

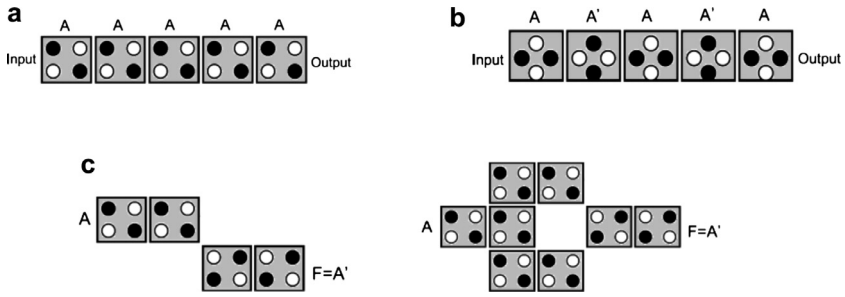

Fig. 2. (a) QCA 90° wire, (b) QCA 45° wire, (c) QCA NOT gate.

(7) Single missing/additional cell based defect analysis for the QCA circuits are performed.
(8) The power dissipated by the proposed QCA layouts is estimated.
(9) The accuracy of all the circuits under thermal randomness is tested and excelled.
(10) The circuits are evaluated based on parameters like logic gate, circuit density and operating speed. The simulation outputs are verified by the truth table.

The paper is structured as follows. Section 2 describes the different devices of QCA. In Section 3, the design and implementation methodology of proposed binary incrementer circuit in QCA platform are demonstrated. In Section 4, the simulation results are verified through truth table. Section 4 also deals with the estimation of dissipated power, defect analysis, quantum cost estimation and design accuracy under thermal randomness. The conclusion is finally summarized in Section 5.

2. QCA devices

In QCA, each QCA cell is represented by using a square structure as shown in Fig. 1a. Each square is prepared with four quantum dots [10]. Every dot can holds only single electron. First two free electrons are pushed into the QCA cell, which are then moved to the diagonal position due to their repulsion within the cell. The arrangement of electrons are used to represent the logic value "0" and logic value "1" as shown in Fig. 1a. The basic device of QCA circuit is majority voter (MV). It consists of five QCA cell as shown in Fig. 1b. The output of majority voter (F_{MV}) depends on its inputs. The logic equation for F_{MV} can be written as $AB + BC + CA$, where A, B, C are the inputs to majority voter [11-12, 14]. By placing one of inputs to zero or one, the majority gate can be utilized as AND gate and OR gate respectively. The layouts are shown in Fig. 1c. The corresponding expressions are shown in Eqs. (1) and (2), respectively.

$$F_{MV}(A, B, 0) = A \cdot B \tag{1}$$

$$F_{MV}(A, B, 1) = A + B \tag{2}$$

In QCA, signal propagation is achieved through QCA wire, which is of two types namely: (1) 90° QCA wire and (2) 45° QCA wire, i.e., inverter chain. In 90° wire, the logic value is same in the entire consecutive cell and in 45° wire; the logic value alternates between each consecutive cell. The different types of QCA wire are shown in Fig. 2a and b respectively. Inverter (IV) is another important logic device used in QCA circuit [14-16]. Two basic ways to achieve inverter in QCA are described in Fig. 2c.

3. Reversible binary incrementer using QCA

Reversible binary incrementer design using QCA is explored in this section. This section is organized as follows. The overview of reversible circuit and binary incrementer circuit are illustrated in Section 3.1. In Section 3.2, QCA based design of Peres gate is demonstrated. Section 3.3 deals with the design of reversible half-adder based on Peres gate and it's realization through QCA. Related works are explored in Section 3.4. Finally, novel n-bit reversible binary incrementer is achieved in Section 3.5.

3.1. Reversible circuit and binary incrementer

Any reversible circuit will meet some basic criteria [17]. The conditions of reversible logic are as follows:

(1) Inputs and outputs must be equal in number.
(2) Input and output has one-to-one mapping between them.
(3) No information is lost.

Binary incrementer is a combinational circuit [18]. It is used to carry out increment microoperation. This circuit adds one to a number stored within register. For example, if a register has a binary value 1000, after increment process, it will be 1001.

3.2. Peres gate

Peres gate (PG) is a reversible logic circuit. It has 3 inputs and 3 outputs as shown in Fig. 3a. The input and output has one-to-one mapping having relation as $P = A$; $Q = A \oplus B$; $R = AB \oplus C$ [19]. The truth table is outlined in Table 1. The quantum cost of Peres gate is 4. The QCA layout of Peres gate is shown in Fig. 3b. The QCA layout is achieved by employing 7 MVs, 4 IVs and 4 clocking zones. The corresponding simulation result is shown in Fig. 3c. The result is confirmed by comparing with Table 1. This verification shows that the proposed circuit works efficiently. The rectangular box indicates the required output bits corresponding to input bits.

Download English Version:

https://daneshyari.com/en/article/460919

Download Persian Version:

https://daneshyari.com/article/460919

Daneshyari.com