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Reconfigurable multicast routing for Networks on Chip

Fatemeh Nasiri [a,*], Hamid Sarbazi-azad [b,c], Ahmad Khademzadeh [d]

[a] Department of Computer Engineering, Science and Research Branch, Islamic Azad University, Ashrafi Esfahani Street, Poonak Sq., Tehran, Iran
[b] Department of Computer Engineering, Sharif University of Technology, Tehran, Iran
[c] School of Computer Science, Institute for Research in Fundamental Sciences (IPM), Tehran, Iran
[d] Iran Telecommunication Research Center Institute, PO Box 3961-14155, Tehran, Iran

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ABSTRACT

Several unicast and multicast routing protocols have been presented for MPSoCs. Multicast protocols in NoCs are used for cache coherency in distributed shared memory systems, replication, barrier synchronization, or clock synchronization. Unicast routing algorithms are not suitable for multicast, as they increase traffic, congestion and deadlock probability. Famous multicast schemes such as tree-based and path-based schemes have been proposed originally for multicomputers and recently adapted to NoCs. In this paper, we propose a switch tree-based multicast scheme, called STBA. This method supports tree construction with a minimum number of routers. Our evaluation results reveal that, for both synthetic and real traffic loads, the proposed scheme outperforms the baseline tree-based routing scheme in a conventional mesh by up to 41% and reduces power consumption by up to 29%.

1. Introduction

Current multi-core systems on chip (SoCs) have extended in size and complexity. Future SoCs will consist of complex integrated components communicating with each other at very high speed rates; besides, the micro-processor industry is moving from single-core to multi-core, and eventually to many-core architectures containing tens to hundreds of identical cores, arranged as chip multiprocessors (CMPs) [1,2]. The industry also targets heterogeneous architectures, since they can provide better performance considering application classes (e.g. multimedia) due to specific mix of IPs (GPPs, DSPs, GPUs). The lack of scalability in bus-based systems, and large area overhead and unpredictability of electrical parameters of point-to-point dedicated links, have excavated researches to propose packet-switched Network on Chip (NoC) architectures to win over complex on-chip communication problems [3]. Topology determines connectivity of NoC nodes while routing determines the path between source and destination. Existing challenges lead researchers to generate customized topology and routing algorithms; furthermore, proper selection of routing protocols can have great impact on performance, message latency, and power consumption. Routing protocols in NoCs can be broadly classified into unicast and multicast: in the unicast communication, a message is sent from a source node to a single destination node; conversely, in multicast communication, a message is sent to a group of destination nodes. Although unicast routing is a special case of multicast routing, it cannot support multicast routing efficiently. Indeed, it can just replicate multiple unicast messages to different destinations. So, multicast communication support is an important issue that determines NoC performance under multicast traffic.

In recent years, multicast routing algorithms have been used for clock synchronization, barrier synchronization, cache coherency, and replication in distributed shared memories. Three famous hardware-based multicast routing methods include unicast-based, tree-based and path-based [4–7]. In the unicast-based scheme, multiple copies of the same message are injected into the network leading to increasing traffic and message latency in the network. In the path-based scheme, one message is forwarded only to the next node on a Hamiltonian path and is delivered to every destination noted in its header. This scheme increases the possibility of injection contention at source node and reduces link sharing and communication parallelism; moreover, it suffers from long message latency for transferring messages. On the other hand, a tree-based routing scheme constructs a minimal spanning tree in which source node is specified as the root node to direct a multicast message down the tree in order to reach all destination nodes. So, a message might be replicated at some intermediate nodes and conducted along multiple outgoing channels to reach subsets of destination nodes. If one branch of tree is blocked, the whole tree is blocked. When branches proceed forward in blocked state, it may cause a message keep many channels for several cycles; therefore,

* Corresponding author.
E-mail address: Fatemeh_nsr@yahoo.com (F. Nasiri).

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it may increase network contention. Therefore, this algorithm is suitable under low injection rates. A solution to overcome this disadvantage of tree-based algorithms is to use reconfigurable NoC. Reconfigurable NoC has switches located at the neighborhood of routers. It has a suitable architecture for handling different traffic flows, so it is proper to construct minimal spanning tree in order to direct multicast traffic.

More precisely, we propose Switch Tree-Based Algorithm (STBA) which uses a reconfigurable platform. STBA uses switches in a reconfigurable network to construct minimal spanning tree with adaptive west first routing algorithm to direct messages from source node as the root to destination nodes. Overlap between trees via switches of the reconfigurable network is not allowed. Ideally, all the trees must be constructed via switches to minimize power consumption and message latency. However, it may not be possible to construct all trees by using switches. Therefore, the constructed tree may consist of switches and routers. In other words, when a minimal spanning tree cannot be constructed with configuration switches purely, we consider constructing the tree as a combination of switches and routers to direct more multicast traffic; afterwards, blocking of branches in the tree is decreased. It means that by bypassing intermediate routers between source and destinations, we can increase performance considerably. For evaluation, we use synthetic and real workloads. Our experimental results show that power and message latency are improved by exploiting STBA scheme compared to tree-based multicast in a conventional mesh.

The rest of the paper is organized as follows. In Section 2, motivation of this research along with a brief review of the tree-based multicast routing algorithms and reconfigurable NoC are described. In Section 3, previous related work is discussed. Section 4 presents the main ideas. We then discuss the experimental results in Section 5, and finally, conclude our work in Section 6.

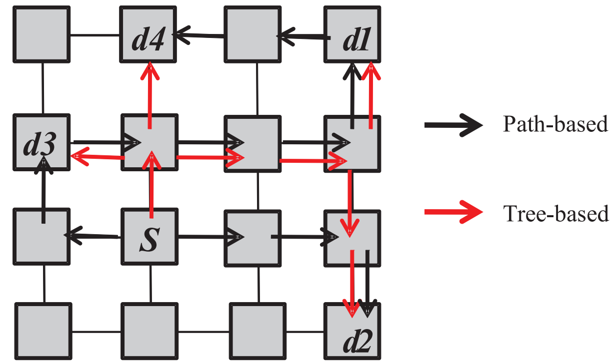

Fig. 1. Tree-based and path-based multicast routing algorithms. Red lines show tree-based multicast routing algorithm and black lines show path-based multicast routing algorithm with a source and 4 destination nodes. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

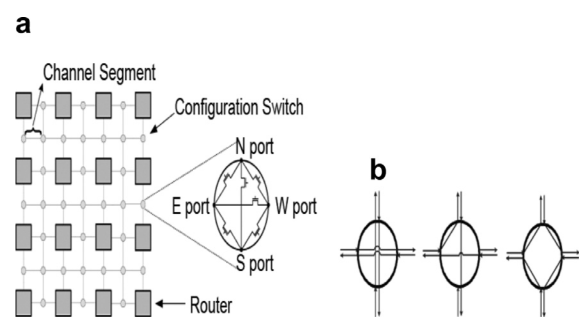

Fig. 2. (a) The reconfigurable NoC architecture and internal structure of configuration switches, (b) three possible switch configurations [12].

2. Preliminaries and motivation

2.1. Multicast routing algorithms

It is intuitive that injecting multiple messages with different number of destinations imposes significant throughput degradation to the NoC [4]. So, multicast routing algorithms are proposed to overcome this issue. As stated earlier, path-based scheme conducts messages from source node to destinations over a Hamiltonian path. It means that based on nodes' labeling, two subnetworks of directed Hamiltonian path, i.e. low-channel and high-channel sub-networks, are clarified in the network. If destinations' label is greater than that of the source label, routing is conducted in high-channel sub-network; otherwise, routing is done in low-channel sub-network. As discussed, path-based is attractive because of its simple hardware design, however, if destination nodes are outspreaded from each other, path-based scheme may suffer from high message latency compared to tree-based scheme; conversely, tree-based multicast routing delivers message along a minimal spanning tree and constructs branches when needed. If one branch is blocked, the whole tree will be also blocked. This situation is more highlighted in the case of high traffic loads. The policies of tree-based and path-based schemes are shown in Fig. 1.

Existence of blocking problem in tree-based multicast schemes motivated us to propose a tree-based method in order to improve NoC's performance by constructing minimal spanning tree with configuration switches in a reconfigurable network. We benefit from bypassing intermediate routers to construct a tree, and decrease branch blocking in the constructed tree.

2.2. Reconfigurable network architecture

As topology is one of the most important architectural factors in NoCs, different topologies have been proposed to reduce power consumption and message latency of NoCs. The reconfigurable topology proposed in [12,13] offers an appropriate tradeoff between design flexibility and area overhead. In addition, routers are not connected directly to each other, but they are connected via switches. These switches, called configuration switches, are shown in Fig. 2. Each square box presents a network node which consists of a processing element and a router. Each circle contains a configuration switch. Fig. 2(a) shows internal structure of configuration switches. It comprises some simple transistor switches that can establish connections between incoming and outgoing links. For the sake of simplicity, only a single connection is depicted between each two ports of a configuration switch in Fig. 2(a); however, there are two connections between each two ports of configuration switch in order to lead the incoming and outgoing sub-links of a bidirectional link. For example, the incoming sub-link of S (south) port can be connected to the outgoing sub-link of some other ports (E port, for example) while the outgoing sub-link of S port is connected to the incoming sub-link of another port (N port, for example). A multiplexer at each output port of the switch can implement the internal connections. Each multiplexer is connected to three input ports, as loop backs are not allowed. Fig. 2(b) shows three possible switch configurations.

An important issue in this topology is the number of consequent channel segments between switches which create long links. These long links in a conventional NoC may decrease NoC clock frequency and as a result, flits cannot traverse via these switches during one cycle. Using repeaters also cannot solve the exceeded delay problem. To overcome this problem, long links should be segmented into fixed length links that are connected by one flit buffers. When the connection between two adjacent nodes consists of two channel segments, the flit buffers should be placed among the configuration switches. Each flit is latched after