Microprocessors and Microsystems 37 (2013) 420–429

Contents lists available at SciVerse ScienceDirect

Microprocessors and Microsystems

journal homepage: www.elsevier.com/locate/micpro

Multi bit random and burst error correction code with crosstalk avoidance for reliable on chip interconnection links

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ARTICLE INFO

Article history:
Available online 28 March 2013

Keywords:
NoC
Triplication error correction
Reliable on-chip-interconnect
DSM noise
Random errors
Burst errors
SEC–DED
Crosstalk
CACs

ABSTRACT

We propose an energy efficient error control code for the on chip interconnection link capable of correcting any type of error patterns including random and burst errors up to five (i.e. 1, 2, 3, 4, and 5 errors). The proposed code is based on single error correction–double error detection (SEC–DED) extended Hamming code and standard triplication error correction scheme. Using single error correction–double error detection (SEC–DED) extended Hamming code and standard triplication error correction scheme a new decoding algorithm is proposed to correct multiple errors up to five in on-chip interconnection link. Triplication error correction scheme provides crosstalk avoidance by reducing the coupling capacitance of the interconnection wire. The proposed code provides high reliability compared to other error control codes. The performance of the proposed code is evaluated for codec area, codec power, codec delay, residual flit error rate, link swing voltage and link power. For the given reliability requirement of 10^{-5} and 10^{-20}, the proposed code achieves low residual flit error rate and low swing voltage. The low swing voltage results in the reduction of the link power consumption up to 68% compared to the existing error control codes for on chip interconnection link. The low residual flit error rate and low link power make the proposed code appropriate for on chip interconnection link.

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1. Introduction

With the shrinking feature size and increasing die size, integration of large number of functional blocks, storage elements and intellectual property (IP) in a single chip increases [1]. As the number of functional blocks in a single chip increases, the bus based communication becomes inefficient in a System-on-Chip (SoC). Networks-on-Chip (NoC) is a paradigm that provides solution to the communication problem in a SoC. In NoC, the functional blocks communicate through routers. Routers are interconnected using interconnection wires [2]. In nano scale technology, due to scaling of supply voltage, increasing interconnect density and faster clock rates, on chip interconnect wires suffer from three major problems. They are: (i) delay; (ii) power consumption; and (iii) reliability [3]. The delay problem is due to capacitive coupling and is called capacitive crosstalk [3–6]. While the gate delay reduces with scaling, the global interconnection wire delay increases. Due to high parasitic capacitance and coupling capacitance, power consumption is increased [7,8]. Moreover, around 20–36% of the total system power is consumed by interconnection network in many NoCs [3]. Due to deep submicron noises (DSM) such as transient errors and electromagnetic interference, on chip interconnect wires are more susceptible to random and burst errors. These errors affect the reliability of the interconnection wires [9,10]. The probability of adjacent multi wire (burst error) error is much higher than the probability of multiple random multi wire (random) errors [10]. Hence detection and correction of random as well as burst error is important to increase the reliability of the NoC interconnect. Thus to have a good performance in the design of on chip interconnection network, delay, power and reliability are the three major issues to be addressed [3].

Low power coding techniques [11,12] have been proposed to reduce the power consumption of the interconnection wire by reducing the switching activity in the interconnection wires. Crosstalk avoidance codes (CACs) [13,14,22–28] are proposed to reduce the delay problem. To increase the reliability, error control codes such as automatic repeat request (ARQ), hybrid ARQ (HARQ) and forward error correction (FEC) have been proposed in [15–18]. Joint crosstalk avoidance and forward error correction schemes [22–28] have been proposed to address the delay and the reliability problems. These techniques avoid crosstalk and correct any error patterns up to three errors only. In [36], the authors correct up to 4 bit errors without using crosstalk avoidance code.

In this paper, to address the delay and reliability problem of NoC interconnect link, we propose combined random and burst error correction code with crosstalk avoidance. The proposed code

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0141-9331/$ - see front matter © 2013 Elsevier B.V. All rights reserved.
http://dx.doi.org/10.1016/j.micpro.2013.03.001

corrects any type of error pattern up to five (i.e. 1, 2, 3, 4, and 5 errors) including random errors, burst error and combination of random and burst errors. This is the first error correction code with crosstalk avoidance to correct random errors (or) burst errors (or) combination of random and burst errors up to five (i.e. 1, 2, 3, 4, and 5 errors). The previous error correction code proposed with crosstalk avoidance for on chip interconnection link corrects up to three errors (i.e. 1, 2 and 3 errors) only. The rest of the paper is organized as follows: Section 2 presents related work in reliability of NoC interconnects. In Section 3, the design of the proposed error correction encoder and decoder is presented. Section 4 presents performance analysis. Finally in Section 5, conclusion is presented.

2. Related work

To increase the performance of the NoC interconnect, many research groups proposed FEC coding and joint error correction coding with crosstalk avoidance. Single error correcting (SEC) Hamming code [17], single error correction and double error detection (SEC–DED) extended Hamming code [18] is used to correct single error and detect double errors. When double errors are detected, HARQ scheme is used to correct the errors. These works have focused only to correct one bit (or) two bit random errors. But, NoC interconnect wires are more vulnerable to multiple random and burst errors because of DSM noise. Hence, more power full error correction schemes are needed to correct multiple random errors as well as burst errors. In [19,20], adaptive error control schemes have been proposed for variable noise environment. In this work, single SEC Hamming code is used to correct single random error in low noise environment and multiple SEC Hamming code to correct multiple random errors in high noise environment. The author has also used multiple SEC Hamming code with interleaving to correct burst errors in high noise environment. In [21], the author use single SEC Hamming code to correct single random error in low noise environment and Hamming product codes with type II HARQ to correct multiple random errors and burst errors in high noise environment. This code does not include crosstalk avoidance with it. Joint crosstalk avoidance and single error/multiple random error correction codes have been proposed [22–29]. Crosstalk avoidance and single error correction (CAC/SEC) like duplicate add parity (DAP) [22], dual rail (DR) [23], boundary shift code (BSC) [24], modified dual rail (MDR) [25] and triplication error correction scheme [29], reduce the coupling capacitance of the on chip interconnect wire from $(1 + 4\lambda)\ C_L$ to $(1 + 2\lambda)\ C_L$ and simultaneously corrects single random error. In [27], the authors propose crosstalk avoidance SEC and two bit burst error detection. When two bit burst error is detected, HARQ retransmission scheme is used to correct the errors. DAP coding scheme is used for triple error correction and quadruple error detection in [28]. In [29], triplication error correction coding scheme and majority decoder are used to correct only single random error.

Previous works proposed for combined crosstalk avoidance and error correction code, have focused only to correct errors of maximum three bits only. The works proposed in [22,26–28] use DAP coding scheme and correct only one, two or three bits errors with crosstalk avoidance. But, the work proposed in this paper corrects any error pattern up to five (i.e. 1, 2, 3, 4, and 5 errors) including combination of random and burst errors and simultaneously avoiding crosstalk between interconnect wires. This is the first error correction code proposed with crosstalk avoidance to correct any error pattern up to five for on chip interconnect link. The proposed error control code is named as Multi Bit Random and Burst Error Correction code with crosstalk avoidance (MBRBEC).

3. Crosstalk avoidance of the proposed MBRBEC code

The proposed MBRBEC code uses triplication error correction scheme [29] to avoid crosstalk. The worst case capacitance of on chip interconnection link is given by $(1 + 4\lambda)\ C_L$, where λ is the ratio of the coupling capacitance to the bulk capacitance and C_L is the output load capacitance. The effective coupling capacitance of on chip interconnection link depends on transition on adjacent wires [30]. The worst case crosstalk happens when two neighbors make transition in opposite direction with respect to the victim wire [20]. Therefore inclusion of CACs simultaneously avoids the transition of a bit in opposite direction in adjacent wires and avoids the worst case transition of a bit pattern 101<=>010 and vice versa. This reduces the switching capacitance from $(1 + 4\lambda)\ C_L$ to $(1 + 2\lambda)\ C_L$. Thus the worst case energy dissipation of the wire is reduced from $(1 + 4\lambda)C_L\alpha V_{dd}^2$ to $(1 + 2\lambda)C_L\alpha V_{dd}^2$, where α is the switching capacitance and V_{dd} is the supply voltage. Thus, an energy saving is achieved in the presence of CACs with decrease in the coupling capacitance [28].

3.1. Design of the proposed MBRBEC encoder

The proposed MBRBEC encoder uses SEC–DED extended Hamming code (39,32) to encode the initial message bits. Triplication error correction scheme is one of the standard error correction schemes used in communication system to correct errors. We propose triplication error correction scheme to correct the errors in on chip interconnection link. Using triplication error correction scheme [29], each of the encoded message bit is triplicated. Thus if the initial SEC–DED extended Hamming code is (n,l), where n is the encoded message and l is the original message, then the final number of bits in the triplication message is $3n$. The triplication of the message bit is used to correct the errors and simultaneously avoids crosstalk.

The minimum Hamming distance of the SEC–DED extended Hamming code is 4. The triplication of the encoded message increases the minimum Hamming distance to 12. Based on information coding theory, the minimum Hamming distance of k can correct $\lfloor (k-1)/2 \rfloor$ errors. Therefore, MBRBEC code can correct up to five errors. The block diagram of the proposed MBRBEC encoder is shown in Fig. 1a and the flow diagram is shown in Fig. 1b.

3.2. Design of the proposed MBRBEC decoder

The proposed MBRBEC decoder utilizes the fact that SEC–DED decoder corrects single error and detects double errors. SEC–DED decoder sometimes detects four errors if the syndrome value is not zero. If the occurrence of four errors produces syndrome value as zero, then SEC–DED decoder will not detect four errors [28]. The complete block diagram of the proposed decoder is shown in Fig. 2a. The received bits are grouped as group A, group B and group C in group separator. The group separator is a simple wired connection that separates the received bits into three groups (Received_A, Received_B, and Received_C) as shown in Fig. 2c. The three received groups are given to the three SEC–DED decoders that compute the syndrome values Syn_A, Syn_B, Syn_C and occurrence of double errors Double error_A, Double error_B, and Double error_C for the three groups. Based on the syndrome value, each SEC–DED decoder corrects the occurrence of single error and detects the occurrence of the double errors in each group. The decoded values (output from three decoders) Decoded_A, Decoded_B, and Decoded_C are given to the multiplexer. The three received groups Received_A, Received_B, Received_C, and Decoded_A, Decoded_B are compared in the comparator as shown in Fig. 2b to generate the signals Received_Not_eql and DecodeA_eql_DecodeB. Received_Not_eql signal

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