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# A low-cost, fault-tolerant and high-performance router architecture for on-chip networks

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ABSTRACT

The router as the main component of on-chip networks has a key role in making connections between the processing cores. Thus, regarding the unreliable silicon, preserving the routers in operational states has a great effect on the network performance. Among different units of a router, the input ports including the buffers have a high fault occurrence probability due to consuming a large portion of a router's area. This paper presents a fault tolerant router architecture which utilizes a new decoupled resource sharing approach for the input ports. The proposed architecture highly improves the overall reliability and network performance against multiple permanent faults in the input ports even incorporating a non-fault tolerant routing algorithm. Furthermore, the new resource sharing approach decreases the packet latencies while the faulty links exist in the network. The experimental results show that all improvements are achieved at the cost of a very low hardware overhead compared to the baseline router while the proposed router architecture reaches to greatest Silicon Protection Factor (SPF) as a metric compared to all previous designs.



## 1. Introduction

In recent years, the number of cores which are able to be integrated into a single chip, as a System-on-Chip (SoC), has been increasing due to the advancement of the silicon processes. As a result, interconnecting tens or hundreds of cores has become one of the major challenges in such systems. Meanwhile, Network-on-Chip (NoC) has become the prime architecture for both homogenous and heterogeneous many-core systems because of having the scalability and high communication bandwidth.

NoC is a structured set of routers or switches that are connected to each other with some point to point links in order to provide a communication backbone to the processing elements (PEs) of the system [1]. Aggressive technology scaling [2] causes NoC designs to have billions of transistors along with many challenges in the fabrication process in deep submicron. One of the major challenges is that some components may be defective in the manufacturing phase. Besides, it is probable that these components fail in the operational phase because of the impact of environmental effects. As a NoC includes many numbers of routers and links, it may involve some faulty components, permanently. If the faulty components are not resolved, they lead to router or link failures and finally the system failure.

It should be noted that transient faults bring about less impact compared to permanent faults due to the fact that they incur temporary effects, and can be resolved by some specific solutions such as [3,4]. To deal with the permanent faults in NoCs, various approaches have been proposed so far. Some of these approaches are based upon node's structure modification [5,6]. Some methods find the replacement paths by using fault tolerant routing algorithms in the network layer [7–9], and most of the remaining methods incorporate some redundancy and modification inside the links [10] or router architectures [11–14].

In on-chip networks, it is evident that router failures are more harmful than link failures since a router has more influence than a link on the routing process because of containing the main functional units of a NoC. Furthermore, a router failure causes its corresponding core or PE to be unreachable which means some resource will be wasted. The faulty routers can be handled by a fault tolerant routing algorithm such as [15] if a failed router is treated as a node with all links assumed faulty after task migration or remapping of the tasks in the system. In addition, a faulty router may be treated as a faulty link, and thus can be handled by many fault tolerant routing algorithms. However, the network performance degradation is rather high.

Among different units of a router, the input ports including the buffers consume most of a router's area and power, and thus are more prone to be faulty. In this paper, new fault tolerant router architecture is presented based on a novel decoupled resource

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sharing in the input ports to improve the router reliability against permanent faults that eventually improve both the overall network reliability and network performance. The proposed router architecture tolerates multiple permanent faults at the cost of minimal and reasonable hardware overhead. Moreover, at the presence of the faulty links, enhancement in the network performance is achieved by reducing the average packet latency. The rest of the paper is organized as follows. In Section 2, the related works are described, and in Section 3 the baseline router architecture is presented. Then, the proposed router architecture is illustrated in Section 4. The experimental results are presented in Section 5, and finally, some conclusions are drawn in Section 6.

## 2. Related works

So far, different fault tolerant router architectures have been proposed. In [16], the authors proposed the BulletProof router that employs different techniques such as Triple Modular Redundancy (TMR) and Error Correcting Codes (ECC) in different design levels of a router to provide fault tolerance. However, a TMR implementation is expensive because it requires at least triple silicon area for each component in a router. Kim et al., [11] presented the RoCo router architecture which enables the router to be decomposed into individual row and column components. Decomposition is facilitated by using decoupled parallel arbiters and smaller crossbars for row and column connections. Since the row and column components are independent from each other, a permanent fault in one of the components does not affect the other component, and the router continues to function in a degraded mode with the fault-free component.

In [17] a new NoC router is proposed that makes use of some inserted default backup paths within the router. These backup paths serve as alternative data-paths inside the router to circumvent failed functional units of the router. Therefore, the connectivity of healthy routers and PEs will be maintained while the faults exist. However, the packet transmission latency increases when the number of faulty routers on the transmission path increases. A hybrid router architecture called Vicis is proposed in [18] that can tolerate different faults at network level and router level by reconfiguration. The faults at the network level are tolerated via an input port swapping algorithm. In addition, an adaptive routing algorithm updates the routing tables to redirect the traffic around faulty links. Within the router, a bypass bus is used to tolerate the failed crossbar, and a low overhead ECC is utilized to tolerate the faulty components on the data-path. Another router architecture [19] called REPAIR utilizes some partial redundancies for the input buffers and the crossbar switch along with ECC modules to tolerate the permanent faults inside the router. Despite the fact that the methods proposed in [18–19] are highly fault tolerant, they require a rather high hardware overhead of 40% to 50%.

In [20] the Enhanced Reliability Aware Virtual Channel architecture (ERAVC) is proposed in which the virtual channels are dynamically allocated in such a way that the input channels being idle because of their faulty neighbor routers are effectively utilized to improve the overall performance. A more complete version of [20] is proposed in [21] which can tolerate both permanent and transient faults. However, as both designs use a type of fully virtual channel sharing in the input ports, they require complex memory control logic and the corresponding overheads, as well. In addition, a fault inside the common multiplexer (MUX) or demultiplexer (DeMUX) of the input ports causes all buffers to be lost, and the router is treated as an isolated faulty router.

A Partial Virtual channel Sharing (PVS) router architecture is proposed in [22] that uses a resource sharing technique to enhance both resource utilization and fault tolerance for the input ports and routing units. The proposed router considers a simple dedicated routing unit for each input port. It shares a set of buffers among input channels, and reduces the network latency even in a fault-free NoC. However, if a fault occurs inside a common DeMUX, all corresponding input ports will fail and cannot be utilized anymore. In [14] an improved router design is presented where some redundancy is incorporated in each pipeline stage of the router to provide better fault tolerance. In fact, this router benefits from redundant components and resource sharing to ensure the fault tolerance in the pipeline stages such as the routing computation, virtual channel allocation and switch allocation. Despite of having a higher reliability compared to the similar designs, the faulty input ports have not been considered in this design besides incurring an obvious latency impact.

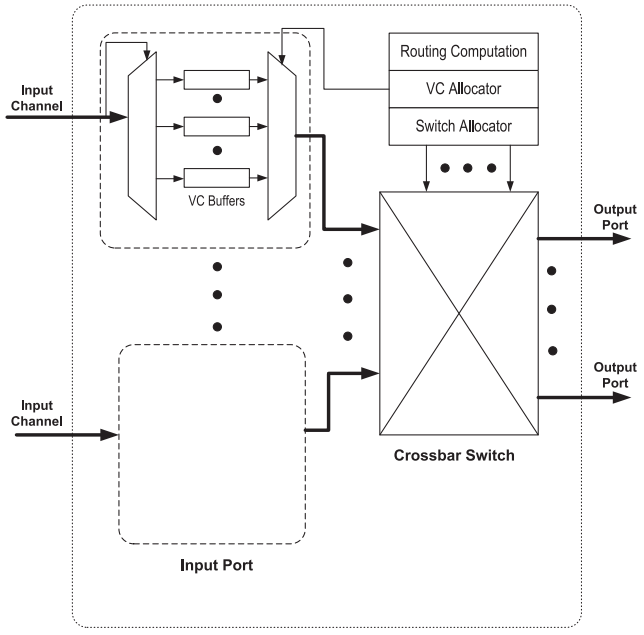


**Fig. 1.** Baseline router architecture.

Investigation of the previous designs reveals that most router designs incur a high area and power consumption overheads. Besides, many designs suffer from a type of weakness in the fault tolerance capability or the network performance. However, in this paper, a very low-cost router architecture utilizing a novel technique for resource sharing in the input ports is presented which results in a higher fault tolerance regards to the overheads compared to the previous designs.

## 3. Baseline router architecture

In the subject of designing fault tolerant routers for on-chip networks, a generic architecture is usually used as the baseline router (Fig. 1). The baseline router consists of five input ports and five output ports. These input/output ports correspond to four main directions (north, south, east, west) and a connection to the local PE through the Network Interface (NI). The baseline router is composed of five functional modules including the Routing Computation (RC) unit, Virtual channel Allocator (VA), Switch Allocator (SA), crossbar switch, and the input ports containing the Virtual Channel (VC) buffers.

According to the wormhole switching, a packet is segmented to the same size flits (flow control information units) for an efficient utilization of input buffers and the crossbar switch. A packet is typically divided into a header flit, payload or data flits, and a tail flit. The header flit is used in the routing process and is also responsible for the resource allocation to the packet. However, the