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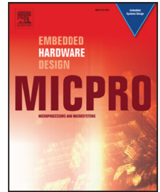

Processor-level reliability simulator for time-dependent gate dielectric breakdown

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ABSTRACT

Time-dependent gate dielectric breakdown (TDDB) is a leading reliability concern for modern microprocessors. In this paper, a framework is proposed to analyze the impact of TDDB on state-of-art microprocessors and to estimate microprocessor lifetimes due to TDDB. Our methodology finds the detailed electrical stress and temperature of each device within a microprocessor system running a variety of standard benchmarks. Combining the electrical stress profiles, thermal profiles, and device-level models, we perform timing analysis on the critical paths of a microprocessor using our methodology to characterize microprocessor performance degradation due to TDDB and to estimate the lifetime distribution of logic blocks. In addition, we study DC noise margins in conventional 6T SRAM cells as a function of TDDB degradation to estimate memory lifetime distributions. The lifetimes of memory blocks are then combined with the lifetimes of logic blocks to provide an estimate of the system lifetime distribution.

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1. Introduction

Increasing operating temperatures and electrical fields, combined with the scaling of dimensions, have contributed to faster aging due to wearout. Not only does this result in the shortening of microprocessor lifetimes, it leads to faster wearout resultant performance degradation with operating time. Microprocessor lifetime is a function of both device and backend wearout. Since previous work has studied the impact of backend wearout mechanisms, bias temperature instability and hot carrier injection on microprocessors [1–5], this paper focuses on time-dependent gate dielectric breakdown (TDDB). TDDB is a failure mechanism in MOSFETs, when the gate dielectric breaks down as a result of long-term application of electric field. The breakdown is caused by the formation of conducting paths through the gate dielectric to the substrate due to electron tunneling currents.

The analysis of TDDB is different than the analysis of backend wearout mechanisms, such as electromigration and stress-induced voiding. Backend wearout mechanisms result in open and short circuits, which cause system failure directly. Evidence indicates that electromigration and stress-induced voiding failures are sudden failures [6,7]. Hence it is sufficient to model the time-to-failure of components of the system and to combine them statistically. TDDB, on the other hand, causes a gradual weakening of the devices. The weakening is both random and a function of stress and temperature. However, unlike backend wearout mechanisms, the relationship between degradation and the circuit performances must be taken into account to determine the lifetime distribution.

Device lifetime is a function of two kinds of stress: electrical and thermal. An increase in either of the two results in decreased device reliability. The increase in device densities has been achieved through a reduction in device dimensions, which means that the devices undergo increased electrical stress during their lifetime. The resulting increase in operating frequency, as well as device densities, has led to greater thermal stress, which also increases with each new generation. A decrease in device reliability and the increase in system complexity translate into systems whose lifetime characterization is both challenging due to the large number of devices that degrade simultaneously and extremely critical.

The physics describing device failure mechanisms has matured as a result of years of refinement to existing theories. However, the extension of these models to large and complex microprocessor systems is not straightforward. Microprocessor system reliability analysis requires techniques to extend the results gathered from small test structures to large complex microprocessors. Such an endeavor requires methods to manage the deluge of data that comes with analyzing large numbers of devices degrading at different rates.

The purpose of this paper is to present a methodology to assess microprocessor lifetimes and circuit performances due to TDDB by developing the link between the device-level wearout models and the circuit performance requirements while taking into account

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realistic use scenarios [8]. The lifetime results are not based on degradation limits selected by process engineers, but instead by the time-to-failure of circuit performances.

Since TDDB is activity and temperature dependent, the proposed framework determines the average electrical stress and temperature of each device within the system by running a variety of standard benchmarks. Microprocessors contain both logic and SRAM components. Hence, both types of blocks are considered in this work.

We combine the electrical stress profiles, thermal profiles and device-level models, and apply statistical timing analysis (incorporating process variations) to characterize microprocessor performance degradation of logic blocks. Similarly, electrical and thermal stress profiles are combined with device-level models to determine the memory cell time-to-failure. The memory cell lifetime distributions are combined, taking into account the use of error correcting codes, to determine the overall memory lifetime. This work on computing the lifetime distributions for both logic and memory enables a designer to make any updates in the design to enhance reliability prior to committing a design to manufacture.

It is well understood that when the gate dielectric layer abruptly loses its insulating properties, it is called hard breakdown (HBD), and HBD can be detected as a large jump in the current vs. time curve. Prior to hard breakdown, TDDB experiences soft breakdown (SBD) where the leakage current in the gate dielectric slightly increases with time, while the gate dielectric still retains its insulation property. SBD is observed as a gradual weakening of the devices. This furthermore can cause failures of the system as the circuit performances degrade when the degradation is sufficient to cause timing errors and to degrade the static noise margins beyond performance specifications. In this work, as in prior work [9], SBD is modeled by inserting a gate-to-source resistance (R_{G2S}) or gate-to-drain resistance (R_{G2D}) in a target gate in order to create the current leakage path in the circuit. The values of the resistance are a function of the number of SBD paths. The number of SBD paths is determined with a percolation model to count the number of conduction paths and the time to soft breakdown (SBD) for each stress scenario. The number of soft breakdown paths translates into a resistance, which in turn impacts timing and memory performances. This paper presents a methodology to determine logic and memory circuit tolerance to soft breakdown events for the first time, in addition to the computation of the corresponding lifetime distributions.

Timing analysis is implemented in [10], including the updating of path selection throughout the aging process. However, prior work has involved smaller circuits and assumptions about stress distributions for each device [10,11]. In this work we have used emulation to handle large systems running actual benchmarks to determine the actual activity of circuits and memory cells under realistic use scenarios. The results from emulation are used to update timing analysis and the analysis of memory performances based on actual usage patterns. Additionally, a methodology to compute the lifetime distribution of memory blocks is presented for the first time, and memory and logic lifetimes are combined to obtain the system lifetime.

This work not only accounts for activity and temperature, but also accounts for the fact that processors are not in operation at all times. Modern processors operate at varying frequencies and voltages in response to demands to conserve power. Our processor examples contain only a single operating mode. Given this constraint, realistic use conditions include the operation mode, standby, and periods of time when the processor is turned off, as illustrated in Fig. 1. This paper takes these use scenarios into account, which are based on large scale user monitoring [8]. These use scenarios are based on actual average usage patterns for different applications. Cycling between states is not considered, since this work focuses on wearout mechanisms affecting the processor, rather than the package.

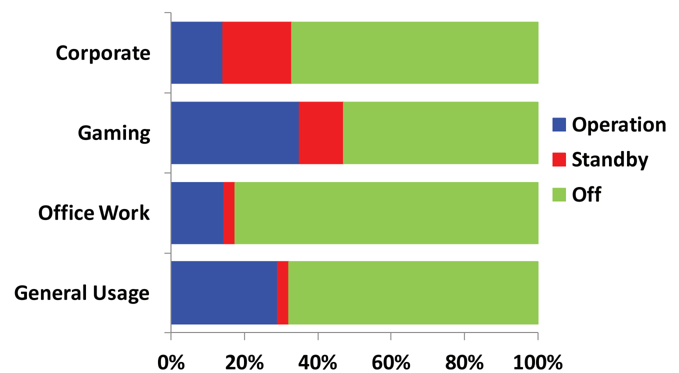

Fig. 1. The use scenarios provided by Intel are shown [8].

The rest of the paper is organized as follows. Section 2 presents the device-level wearout models that we have used in this study. Section 3 gives the overview of our system-level aging assessment framework, describing the methodology to determine model parameters through FPGA emulation. Section 4 describes our methodology to evaluate performance degradation of a microprocessor due to TDDB and presents the degradation and lifetime results for logic blocks of the microprocessor. In Section 5, we present analysis of SRAM noise margins under TDDB degradation and estimate SRAM lifetime. Section 6 combines the lifetimes of memory and logic blocks together. Section 7 determines variation in lifetime as a function of supply voltage and ambient temperature, and Section 7 concludes the paper.

2. Device-level wearout models

We first model TDDB at the device level and then abstract the models to the system level. TDDB is one of the key reliability issues for CMOS devices. Stress induced leakage current (SILC) is induced by trap-assisted tunneling mechanisms where electrons pass from the cathode to the anode via defect sites (neutral traps) in the gate dielectric by the electrical field [12–15]. When the gate dielectric experiences partial breakdown, it is known as soft breakdown (SBD) [12,16].

Experimental observations indicate that the mean time to failure is a function of the total gate oxide surface area, temperature, and gate voltage due to the weakest-link character of gate dielectric breakdown [17]. The conventional model provides a time-to-failure for HBD, as a Weibull distribution with two parameters, η, and the shape parameter, β, where [18]

$$\eta = A\left(\frac{1}{WL}\right)^{1/\beta} \frac{V_G^{a+bT}}{\alpha} e^{-1/\beta} \exp\left(\frac{c}{T} + \frac{d}{T^2}\right) \quad (1)$$

and where W and L are device width and length, respectively, α is the fraction of time that the gate is under stress, T is temperature, V_G is the gate voltage, and $a, b, c, d,$ and A are fitting constants.

However, circuits may fail prior to HBD, due to SBD. To determine the impact of SBD it is important to study the degradation process to understand when and if circuits fail due to SBD. Circuits have been known to operate during breakdown [19]. In order to model circuit performance degradation under SBD, time-dependent resistance models [9,20] and time-dependent leakage current models [21] have been proposed for SPICE simulation. This work uses time-dependent resistance models.

Using emulation, described in the next section, the devices are partitioned into groups that experience equivalent stress and temperature. More specifically, for an nMOS device, the time under stress is the time that the gate has the supply voltage applied. This time

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