Transition delay fault simulation with parallel critical path back-tracing and 7-valued algebra

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ABSTRACT

A new method is presented for simulating of Transition Delay Faults (TDF) based on the parallel exact critical path tracing for Stuck-at Fault (SAF) analysis and subsequent TDF reasoning. A method is proposed to extend the TDF model, traditionally considered as a class of robustly tested delay faults, to a class of TDFs with extended detection conditions. Three known fault classes of delay fault sensitization are considered: robust, non-robust and functional sensitization of delay faults. Additionally, a new fourth fault class is introduced, called non-robust functionally sensitized delay fault. A novel fault analysis algorithm based on 7-valued algebra is presented, which delivers the fault coverage for all mentioned four types of TDFs.

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1. Introduction

The purpose of delay testing is to ascertain that manufactured digital circuits meet their timing specifications. Delay faults can be modeled in different ways, among which the most common models are Transition Delay Fault (TDF) model [1], and path delay fault (PDF) model [2]. The TDF model captures large delay defects that affect single locations in the circuit whereas the PDF model captures small delays, such that each one by itself may not cause the circuit to fail, but their cumulative effect along a path from inputs to outputs may result in faulty behavior. The TDF is as well used as a logic model for stuck-open faults in CMOS circuits, which either suppress or delay the occurrence of certain transitions [3].

The main advantage of the TDF model is the linearity of the number of faults in terms of the number of connections in gate-level circuits. Another advantage is that the stuck-at-fault (SAF) test generation and fault simulation tools can be directly used for handling TDFs. The disadvantage of TDFs is that the expectation that the delay fault in a single location is large enough for propagating up to the observation points might not be realistic. On the other hand, the disadvantages of the PDF model is that the number of paths in circuits is huge, the number of robustly testable paths is in general very small, and as shown in [4], the non-robust tests may not detect delays in certain situations where

the cumulative effect of small delays would be sufficient to be tested non-robustly.

In [4,5] a novel *Transition Path Delay Fault* (TPDF) model was proposed where the ideas of TDF and PDF models are combined to improve the capability of TDFs to detect the delays by combining tests for TDFs along the target paths.

In [6] a new TDF model is proposed called *As Late As Possible Transition Fault* (ALAPTF). The model aims at detecting cumulatively smaller delays, which will be missed by both the traditional TDF and the PDF models. The model makes sure that each transition is launched as late as possible at the TDF site, accumulating the small delay defects along its way.

Both approaches [4] and [6] are based on the idea of creating paths along which the TDFs are consecutively tested.

In both approaches we need to have continuous activated paths or segments of paths along which the TDF will robustly propagate. In general, such paths may be missing, or it may be difficult to create paths along which all the TDFs are detected. In these cases, it may be reasonable to alleviate the constraints on consecutive propagation of TDFs robustly along the tested path, so that in some gates or segments the TDFs may propagate non-robustly or along discontinuous paths.

In [4], it was shown that a test for TPDF corresponds to a type of strong non-robust test [7] for a conventional PDF associated with the same path, however, with the difference that the TPDF test additionally detects the TDFs on every line of the path.

On the other hand, a strong non-robust test satisfies the weak non-robust propagation conditions [7], but not the opposite. As shown in [8], this results in a large gap in the number of detectable

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faults between TPDFs as defined in [4] and conventional PDFs when the weak non-robust propagation conditions are used for them. To bridge this gap, in [8], the detection conditions for TPDFs used in [4] were extended with hazard-based detection conditions for transition faults defined in [9]. When the hazard-based detection conditions are allowed for the transition faults included in a TPDF, it is not necessary to create transitions on every line of the path, rather it is also possible for lines on the path to have hazards. When some of the TDFs associated with a TPDF are detected under the hazard-based detection conditions, the resulting test will be a type of weak non-robust test.

In this paper, we further alleviate the conditions of detecting TDFs in addition to the hazard-based conditions (let us call them non-robust detection conditions for TDFs). We introduce into the detection conditions for TDFs so called *functional sensitization* [7] to handle multiple TDFs and a new type of conditions that we call *non-robust functional sensitization* conditions which allow multiple TDF detection in hazard-based conditions. To determine the detectability of TDFs under mentioned conditions, we introduce 7-valued algebra which will support SAF simulation and allows to classify all the detected TDFs into the classes of robustly detected, non-robustly detected, detected under robust functional sensitization conditions, or under non-robust functional sensitization conditions.

We carry out the TDF simulation in two phases: traditional SAF simulation and additional check which conditions needed for TDF detection are satisfied.

SAF simulation can be carried out in different ways: by parallel pattern single fault propagation [10], critical path tracing [11], deductive [12], or concurrent [13] fault simulation. The last three approaches are based on logic reasoning rather than simulation, and hence, are very powerful since all the detectable faults are calculated by a single run of the current test pattern. What the listed methods cannot do is to produce reasoning for many test patterns in parallel.

The Critical Path Tracing (CPT) approach [11] consists of simulating the fault-free circuit and using the computed signal values for back-tracing of all sensitized paths from primary outputs to primary inputs, to determine all the faults detectable by the given test pattern. The back-trace continues until the paths become non-sensitive or end at network primary inputs. Faults on the sensitive (critical) paths are detectable by the test. In the conventional CPT approach the detectable faults are found by a single run, however the precise results are only guaranteed in fan-out free circuits.

A modified critical path tracing technique that is linear time, exact, and complete was proposed in [14]. However, the rule based strategy used in this approach does not allow simultaneous parallel analysis of many patterns. Parallel critical path backward tracing in fan-out free regions combined with parallel simulation of stem faults was investigated in [15]. In [16], the concept of exact parallel critical path tracing was generalized for SAF cover analysis beyond the fan-out free regions, and in [17], the method was extended for simulation of a large fault class called X-fault.

In this paper we adjust the method proposed in [17] for parallel critical path tracing of TDFs, and we extend the detection conditions for TDFs compared to that proposed in [8,9]. Both phases of TDF simulation will be carried out by critical path backward tracing, the phase of SAF analysis is carried out in parallel for many patterns simultaneously, and the TDF type analysis is carried out pattern by pattern using the 7-valued algebra developed in the paper.

The organization of the paper is as follows. First, in Section 2, the concept of fast parallel critical path tracing method for calculating the detection of SAFs is described. In Section 3, an extension of the class of TDF faults regarding the sensitization conditions is introduced and explained. Section 4 presents a novel 7-valued algebra for determining the detectability of different types of TDFs, and in Section 5 a general procedure for novel TDF simulation is described. Section 6 presents experimental results, and Section 5 concludes the paper.

2. SAF simulation with critical path tracing

In the first phase of TDF simulation we determine the detected SAF faults in the circuit for the given set of test patterns. For this purpose we use the idea of parallel backward critical path tracing used in [16,17]. In the following, the method of SAF simulation based on this idea is shortly described.

Consider a network of Fan-out-Free Regions (FFR) where each FFR is represented as a Boolean function.

$$y = F(x_1, \ldots, x_i, x_j, \ldots, x_n) = F(X),$$

and $X = x_1, x_2, \ldots, x_n$ is the input vector of the FFR. Such a network of five FFRs is represented in Fig. 1. Let

- X_k denote the vector of input variables of the k-th FFR,
- z_k denote the internal fan-out stem variables (outputs of FFRs) with z_{kj} as fan-out branch variables for z_k (inputs of FFRs), and
- y denote the output variables of the circuit.

The task of SAF simulation can be referred to calculation of partial Boolean derivatives: if $\partial y/\partial x_j = 1$ then the fault is propagated from x_j to y. The calculation of derivatives can be performed in parallel for a subset of test patterns, so that each bit in a computer word will correspond to one test pattern. In order to extend the parallel critical path tracing beyond the fan-out free regions we use the concept of partial Boolean differentials [18].

Consider an FFR F, where a group of paths is re-converging from the same node x, as shown in Fig. 2. Denote the Boolean function that represents the FFR subcircuit F as $y = F(x_1, \ldots, x_i, x_j, \ldots, x_n)$.

Assume that the input variables $x_1, \ldots, x_i$ of the FFR F are connected to the fan-out stem x via other FFRs represented by Boolean functions

$$x_1 = f_1(x, X_1), \ldots, x_i = f_i(x, X_i),$$

where the variables of vectors X_i correspond to the nodes in the circuit which do not have paths to x. Then all possible fault propagation conditions from x to y can be described by full Boolean differential:

$$dy = dF$$
$$= y \oplus F((x_1 \oplus dx_1), \ldots, (x_i \oplus dx_i), (x_j \oplus dx_j), \ldots, (x_n \oplus dx_n)) \quad (1)$$

where the Boolean variables dx and dy denote the erroneous changes of the values of x and y, respectively, caused by a propagated fault. By dx we denote the change of the value of x because of the influence of a fault at x, and $dy = 1$ if some erroneous change of the values of arguments of the function (1) causes the change of the value of y, otherwise $dy = 0$.
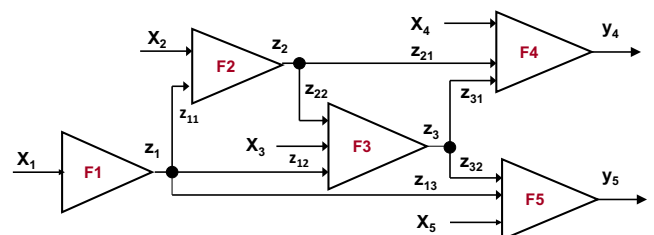

Fig. 1. Combinational circuit with five FFRs.