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100-Gb/s and beyond transceiver technologies

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ABSTRACT

First generation 100-Gb/s Ethernet transceiver architecture, standards and components are presented. Second generation 100-Gb/s architecture, standards and enabling photonic integration component technology are then described. Extension of this technology is shown to support cost effective 400-Gb/s Ethernet interfaces. The next OTN data rate then also becomes 400-Gb/s to efficiently carry a 400-Gb/s Ethernet payload. Further data rate increase to $\geqslant$1-Tb/s is not possible with existing technology, and will require completely new technology R&D effort.

1. Introduction

Optical Ethernet interfaces are the physical layer of the Local Area Network (LAN) communications protocol for sending data over fiber optic cable. It is used for connecting internet servers and switches, inside equipment racks, within data-centers, and between metro data-centers. Today the most widely used LAN data rate is 1-Gb/s, with high adoption of the next data rate; 10-Gb/s. Interfaces at these rates use duplex SMF (Single Mode Fiber) and duplex MMF (Multi Mode Fiber) and are based on single laser Non Return to Zero (NRZ) technology. However, these rates are insufficient to support core networking requirements, such as switching, routing, and aggregation in large data centers, internet exchanges and service provider peering points, and high bandwidth applications, such as video on demand and high performance computing environments. This article discusses 100-Gb/s and beyond Ethernet optical interfaces based on duplex SMF Wavelength Division Multiplexing (WDM) and parallel MMF Multi-fiber Push On (MPO) technology.

Since the determination of the number of lanes and per lane GBaud to create a 100-Gb/s rate has been and continues to be subject of considerable industry debate, an analysis is included in an Appendix A showing how to calculate the maximum feasible Gbaud based on laser and IC figures of merit obtained for mainstream production processes.

2. First Generation 100-Gb/s Ethernet transceivers

First Generation (Gen1) 100G-Gb/s Ethernet transceiver architectures were driven by demand for quick time to market delivery of interoperable modules from multiple optics suppliers. Detailed descriptions of Gen1 module implementations are found in Ref. [9].

2.1. Gen1 100-Gb/s SMF

Gen1 100-Gb/s SMF Ethernet transceivers use discrete optical components based on established optical technologies that enabled low risk development.

2.1.1. Architecture

Fig. 1 shows the architecture of a Gen1 100-Gb/s duplex SMF Ethernet transceiver. It supports reaches up to 10 km and is referred to as 100GBASE-LR4. This architecture can be extended to support reaches up to 40 km, through the addition of a Semiconductor Optical Amplifier (SOA) in front of the receiver, referred to as 100GBASE-ER4. These optical interfaces are specified by the Institute of Electrical and Electronics Engineers (IEEE) in Ref. [1].

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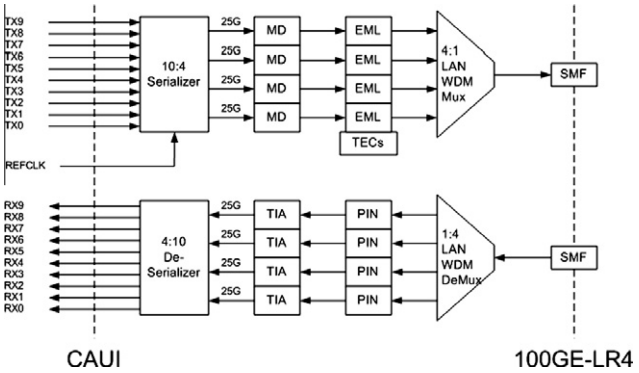

Fig. 1. The 100-Gb/s Gen1 10 km duplex SMF WDM transceiver architecture.

Fig. 2. CFP module.

The lane rate of the electrical interface is 10-Gb/s, determined by I/O rates in mainstream CMOS technologies used for the Media Access Controller (MAC) IC, which connects to the 100-Gb/s optical transceiver. The 10 × 10-Gb/s electrical interface is referred to as CAUI (100-Gb/s Attachment Unit Interface) and is also defined in [1].

2.1.2. Components

The transmitter uses four Modulator Drivers (MDs) and four O-band discrete cooled Electro-absorption Modulator Lasers (EMLs) connected with fiber to WDM multiplexer (mux) which combines the four wavelengths. The optical lane rate is 25-Gb/s and uses low cost NRZ modulation. The four lanes are wavelength division multiplexed over a single fiber in each transmission direction, i.e. duplex. The exact optical lane grid is referred to as LAN WDM, and is listed in Table 1. It is located near the zero Chromatic Dispersion (CD) wavelength of standard SMF.

Translation between the 10-Gb/s and 25-Gb/s lane rates uses 10:4 Serializer De-serializer (SerDes) ICs, alternately referred to as Gearbox ICs. An example of a single chip 65 nm CMOS 2 W IC implementation is found in Ref. [8]. The receiver uses WDM demultiplexer (demux), four PINs (p-intrinsic-n) photodiodes, and four Trans-Impedance Amplifiers (TIAs). A Limiting Amplifier (LA) function is either part of the TIAs or SerDes ICs. For 40 km reaches, a SOA is in front of the receiver.

2.1.3. Module

The transceiver is packaged in the CFP (100-Gb/s Form-factor Pluggable) module, as specified in the CFP Multi-Source Agreement (MSA) [2]. An example module is shown in Fig. 2. The actual size is 82 × 145 × 13.6 mm. To minimize cost, surface-mount components and Printed Circuit Board (PCB) transmission-line RF interconnect is used internally. The module is half the 300-pin MSA module size used to package Gen1 10-Gb/s and 40-Gb/s transceivers 10 years earlier.

2.1.4. Deployment

The 100-Gb/s SMF CFP modules have been reported by multiple optics suppliers in 2010. Finisar modules were used in the first Coherent 100G DWDM trials at Verizon [3]. Opnext discussed their modules in Ref. [4]. Other suppliers are expected to publically present their modules in 2011.

Table 1
IEEE 802.3 100-Gb/s LAN WDM optical grid.

Lane	Center frequency (THz)	Center wavelength (nm)	Wavelength range (nm)
L0	231.4	1295.56	1294.53–1296.59
L1	230.6	1300.05	1299.02–1301.09
L2	229.8	1304.58	1303.54–1305.63
L3	229.0	1309.14	1308.09–1310.19

2.2. Gen1 100-Gb/s MMF

Gen1 100-Gb/s parallel MMF Ethernet transceivers are based on extending 10-Gb/single channel MMF technology to ten parallel channels.

2.2.1. Architecture

Fig. 3 shows the architecture of a Gen1 100-Gb/s parallel MMF Ethernet transceiver. It supports reaches up to 100 m on OM3 MMF, and is referred to as 100GBASE-SR10, specified by the IEEE in Ref. [1]. This architecture can be extended to support reaches up to 150 m through the use of OM4 MMF. The architecture uses a single 24-fiber ribbon cable terminated by MPO connector based around the Mechanical Transfer (MT) ferrule [11].

The lane rate of the electrical interface is 10-Gb/s. The CDR retimed 10 × 10-Gb/s electrical interface is referred to as CAUI. The un-retimed 10 × 10-Gb/s electrical interface is referred to as CPPI (100-Gb/s Physical Medium Dependant Service Interface,) and both are defined in Ref. [1].

2.2.2. Components

The optical lane rate is 10-Gb/s and uses low cost NRZ modulation. Each data lane uses a dedicated single fiber in each transmission direction. The cable has 24 OM3 (or OM4) MMF, 12 for TX direction and 12 for RX direction. For Ethernet applications, only 10 fibers are used in each direction. All links are at 850 nm.

Since the electrical and optical I/O data rate is the same, no rate conversion IC is required. The transmitter uses 850-nm Vertical-Cavity Surface-Emitting Laser (VCSEL) array, and costs significantly less than SMF edge-emitting EMLs or Distributed Feedback (DFB) lasers. Arrays of 12 × 10-Gb/s PIN diodes are fabricated using the same process as single vertically illuminated 10-Gb/s PIN diodes. The 10G-Gb/s LD and TIA arrays use the same technology as single components except for the multi-channel integration.

2.2.3. Module

When implemented in the CFP module, retiming CDRs are required to support the CAUI electrical interface. This permits interchangeability with SMF transceivers. Eliminating the CDRs leads to lower cost and smaller size CXP (100-Gb/s Extended capability Pluggable) module (about 15% the size of CFP), which is specified around the CXP host connector by the InfiniBand (IB) Trade Association [10]. An example module is shown in Fig. 4. The size is 24 × 51 × 14 mm.