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# Improvement of cluster-based Mesh FPGA architecture using novel hierarchical interconnect topology and long routing wires

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ABSTRACT

This paper presents an improved interconnect network for Mesh of Clusters (MoC) Field-Programmable Gate Array (FPGA) architecture. Proposed architecture has a depopulated intra-cluster interconnect with flexible Rent's parameter. It presents new multi-levels Switch Box (SB) interconnect which unifies a downward and an upward unidirectional networks based on the Butterfly-Fat-Tree (BFT) topology. To improve the routability of proposed MoC-based FPGA, long routing segments are introduced as a function of channel width with adjustable span. Compared to basic Versatile Place and Route (VPR) Mesh architecture, a saving of 32% of area and 30% of power was achieved with proposed MoC-based architecture. Based on analytical and experimental methods, we identified and explored architecture parameters that control the interconnect flexibility of the proposed MoC-based FPGA such as Rent's parameter, cluster size, Look-Up-Table (LUT) size, long wires span and percentage. Experimental results show that architecture with LUT size 4 and Cluster arity 8 is the best trade-off between power consumption and density. It can also be noted that in general long wires span equal to 4 and percentage between 20% and 30% produce most efficient results in terms of density and power.



## 1. Introduction

Today, Field Programmable Gate Arrays (FPGAs) are widely used in the computational devices domain which was originally dominated by ASICs. FPGA design big challenge is to find a good trade-off between flexibility and performance. In fact, homogeneous FPGA interconnection architecture occupies up to 90% of the total area and plays major factor behind power dissipation [1]. To make FPGAs more efficient, we need to explore new interconnect topologies and new FPGA architectures. Modern Mesh FPGA architectures are based on a clustered architecture where several Look-Up-Tables (LUTs) are grouped together to act as a Configurable Logic Block (CLB) or also called cluster.

Experiments show that using these Mesh of Clusters (MoC) architectures allows exploiting signal sharing among LUTs locally and then improving overall performance of the FPGA [2]. The best characterization to date which empirically estimates interconnect requirements is Rent's rule [3]. Rent's rule can be applied as follows to MoC-based cluster architecture: $IO = c^* k^p$ where $IO$ is the number of inputs/outputs of the cluster, $c$ is the number of inputs/outputs of a Logic Block (LB), $k$ is the cluster arity and $p$ is the Rent's parameter. Intuitively, $p$quantifies the locality of interconnect requirements and its value is generally bounded by 0 and 1. It has small value when most connections are purely local and only few of them come in from the exterior of the cluster. This parameter is used to qualify and control both; architecture clusters bandwidth (architecture Rent's parameter) and design clustering characteristics (design Rent's parameter). The latter is driven by the allowed number of inputs when design instances are grouped by T-VPack [4] to create clusters. We can distinguish two families of MoC-based FPGAs:

- A Versatile Place and Route (VPR) interconnect [5] which has a sparsely populated Connection Block (CB) and a fully populated intra-cluster crossbar with low Rent's parameter (small inputs bandwidth). The fully populated intra-cluster crossbar is simple and ensures a complete local routability, but it takes no advantage of the logical equivalency of LUT inputs and induces a significant area overhead.
- An improved VPR-style interconnect was proposed by Feng in [6]. He investigated joint optimization of CBs and intra-cluster crossbars depopulation while using a high Rent's parameter ($p = 1$). He achieved an area saving of 28%. However, he optimized only connection of external signals to LB inputs and kept the use of a

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full crossbar to connect feedbacks (LB outputs) to LB inputs, which can be very penalizing. In addition, he did not experiment neither new Switch Boxes (SBs) topologies nor lower clusters Rent's parameter.

In this paper, we propose an improved MoC-based architecture with adjustable long routing wires. Proposed architecture has a new hierarchical SB and depopulated intra-cluster interconnect with flexible Rent's parameter. The objective of this work is to explore the effect on performance of architecture and design Rent's parameters, cluster size, LUT size and long wires percentage and span. Then, we analyse how they interact in order to balance different trade-offs and satisfy application constraints. In order to compare and evaluate various architectures, we rely on two different methods which are analytical method based on Rent's rule modelling and experimental method based on benchmarks circuits implementation. A set of CAD tools to map circuits on the proposed architecture are developed. We used metrics models to explore architectures efficiency in terms of power consumption, area and delay.

The remaining of this paper is organized as follows. Section 2 presents the proposed MoC-based FPGA architecture. Section 3 presents the used exploration methodology and introduces the notion and difference between architecture and design Rent's parameters. Section 4 details the experimentation platform. The metrics models to estimate power consumption, area and delay are presented in Section 5. Experimental results are discussed in Sections 6 and 7.

## 2. Proposed MoC-based FPGA architecture overview

In [7], authors presented a Tree-based architecture which contains a downward network based on the Butterfly-Fat-Tree (BFT) topology and an upward network using hierarchy. They showed that the Tree-based architecture reduces the interconnect area by 56% compared to VPR Mesh architecture. However, they noticed that this architecture is penalizing in terms of physical layout generation. It does not support scalability and does not fit to a planar chip structure. In addition, wire length increases exponentially with higher hierarchical levels [8]. In this work, we propose to cut long wires by moving from Tree to Mesh topology. Inspired from the Tree topology, we propose an improved MoC-based architecture with new hierarchical SBs and depopulated intra-cluster interconnect. This architecture is a mesh of clusters placed into regular 2D grid and connected with hierarchical SBs.

### 2.1. Cluster architecture

Each cluster contains local LBs connected with a depopulated local switch block. Each LB consists of a 4-input LUT and a Flip-Flop (FF). Fig. 1 illustrates an example of cluster with 8 LBs. The depopulated local switch block is divided into Mini Switch Blocks (MSBs). The local interconnect is composed of a downward network and an upward network. The downward network is based on the BFT topology which connects Downward MSBs (DMSBs) outputs to LBs inputs. Each DMSB connects each LB in only one input. The upward network connects LB outputs to an Upward MSB (UMSB) and allows all LBs outputs to reach all DMSBs and cluster outputs. Thus, LBs inside the same CLB are equivalent and their ordering has no impact on routing quality.

$$Nb\_DMSB(CLB) = Nb\_inputs(LB)$$

$$Nb\_DMSB\_inputs(CLB) = \frac{Nb\_inputs(CLB) + Nb\_UMSB\_outputs(CLB)}{Nb\_DMSB(CLB)}$$

$$Nb\_DMSB\_outputs(CLB) = Cluster\_size$$

$$Nb\_UMSB\_inputs(CLB) = Cluster\_size$$

$$Nb\_UMSB\_outputs(CLB) = Cluster\_size$$

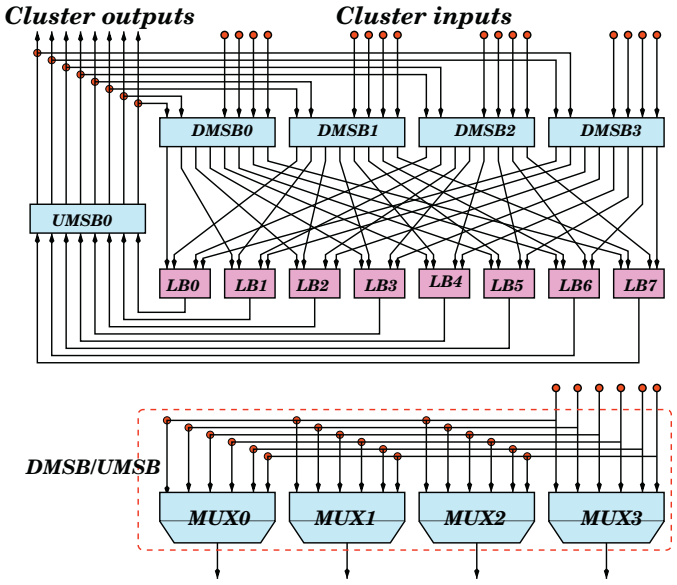


**Fig. 1.** Cluster interconnect with 8 LBs and architecture of the interconnect crossbar.

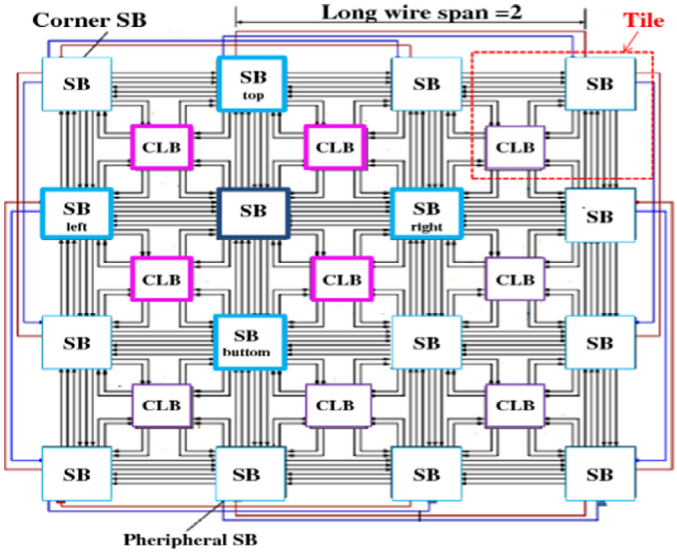


**Fig. 2.** A 4 × 4 array of MoC-based FPGA architecture with long wires with span of 2.

### 2.2. Mesh routing interconnect

Conventional Mesh based FPGA architectures use SBs to connect horizontal and vertical adjacent routing channels and use CBs to connect channel tracks to cluster inputs and outputs. In the proposed mesh routing interconnect, a new multi-levels interconnect of the SB is proposed to connect horizontal and vertical adjacent routing channels and also to connect clusters inputs/outputs to adjacent routing channels. Additional long routing segments which span multiple SBs in every row and column are used in order to improve the flexibility and routability. The number of long wire segments included in each SBs is a function of channel width. The long wire span and number can be adjusted based on the design requirements. As illustrated in Fig. 2, each cluster is connected to 4 adjacent SBs. Fig. 3 shows a detailed view of the interconnect of a SB and a global view of the 4 adjacent SBs (Top, Bottom, Right, Left) and the 4 adjacent clusters (A, B, C, D) highlighted in Fig. 2. Similarly to cluster, the SB has a multilevel topology including 3 main Boxes organized as follows: