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Fuzzy logic based energy and throughput aware design space exploration for MPSoCs

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ABSTRACT

Multicore architectures were introduced to mitigate the issue of increase in power dissipation with clock frequency. Introduction of deeper pipelines, speculative threading etc. for single core systems were not able to bring much increase in performance as compared to their associated power overhead. However for multicore architectures performance scaling with number of cores has always been a challenge. The Amdahl's law shows that the theoretical maximum speedup of a multicore architecture is not even close to the multiple of number of cores. With less amount of code in parallel having more number of cores for an application might just contribute in greater power dissipation instead of bringing some performance advantage. Therefore there is a need of an adaptive multicore architecture that can be tailored for the application in use for higher energy efficiency. In this paper a fuzzy logic based design space exploration technique is presented that is targeted to optimize a multicore architecture according to the workload requirements in order to achieve optimum balance between throughput and energy of the system.

1. Introduction

Traditional design flows for architecture exploration rely heavily either on earlier experiences or domain level expertise of the system architect. This can often result in sub-optimal designs, consequently resulting in sub-optimal performance. Since the scaling of technology, and the advent of multicore architectures has resulted in design spaces that are larger and too complex to be handled by intuitive methods. Consequently, there arises a need of automatic and intelligent schemes to systematically explore the design parameters to find an optimum balance in terms of a particular design goal (such as Energy and Throughput) for specific applications [1]. This process is termed as Design Space Exploration (DSE) [2]. A Design Space is composed of two main parts, i.e. (1) Problem Space and (2) Solution Space. The Problem Space is defined as the parameters that are not ultimate design objectives but rather natural characteristics of the design space effecting the performance metric, whereas the Solutions Space represents the primary objectives of the DSE process, e.g. throughput and energy consumption.

Multicore architectures are rapidly emerging as an important design paradigm for both high performance and embedded processing. These architectures have often been investigated and designed in order to achieve a greater throughput combined with reduced energy consumption [3]. However several issues related to resource sharing on the chip can have a negative impact on the performance of an application and therefore may result in decreased performance [4]. A large body of research now focuses on reconfigurable multicore architectures in order to support DSE algorithms to find optimal solutions for improved energy and throughput balance [5–7]. As a result of on-going research several online and offline DSE techniques and algorithm have been proposed for hardware adaptation [8–10].

Generally, offline DSE techniques aim to optimize the system at design time and therefore contain strategies that are not suitable for runtime implementation for one or more of the following interdependent reasons: (1) requirement of a large number of iterations through simulations, (2) higher complexity, and (3) involvement of large amount of calculations. This paper presents a novel fuzzy logic based design space exploration scheme [11–13] suitable for online application, targeted for Multiprocessor System on-Chips (MPSoCs) to find an optimum balance between power and performance. The main contributions of this work are as follows:

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- A fuzzy logic-based robust DSE technique that can be implemented at runtime for reconfigurable architectures.
- A proposed expert system based (i.e. using expert knowledge-based) scheme for energy efficiency that is independent of sophisticated analytical models.
- A proposed technique that does not require a large number of iterations, and the solution converges in less than 5 iteration for most of the cases shown.

Overall, this paper offers insights on the use of Fuzzy Logic for MPSoC design space exploration to strike a balance on energy consumption and throughput and validates its robustness through analysis of results using multicore benchmarks. Advantages of applying fuzzy control in DSE process are, that it is parameter insensitive, provides fast convergence, accepts noisy and inaccurate signals, and can produce overall good if not the optimal results [14]. Given the importance of energy efficiency in current and future multicore systems, these contributions provide an alternative and straightforward approach to address the issue.

The remainder of the paper is divided into four sections. The following section provides a comparison and review of related wok. The Section 3 gives an overview of the proposed system architecture including the target MPSoC, the Fuzzy Logic based Design Space Exploration (DSE) Engine, benchmarks used and simulation setup. The Section 4 discusses the results, and Section 5 concludes the paper.

2. Related work

In this section, research work related to the proposed design space exploration methodology is discussed and compared. Generally, the DSE techniques can be classified into three main categories according to the design space search criterion [2]: i.e. (1) Exhaustive evaluation of every design point, (2) Random search, and (3) Heuristic search mechanisms involving knowledge of the design space. The result of the above mentioned search techniques, i.e. the candidate configurations are then analyzed using simulations or analytical models.

1. **Exhaustive evaluation of every design point:** This technique involves evaluation of all possible combination of problem space. This method is useful only in situations where the size of design space is very small, for large designs this method is prohibitive due to the latency involved in such unguided search processes. The examples of exhaustive search based DSE are discussed in [15–17].
2. **Random search:** Random search is highly desirable where exhaustive search is not possible due to large design space. Schemes based on Monte Carlo approximations [18], Simulated Annealing [19,20], and Tabu Search [21,22] fall under this category.
3. **Heuristic search mechanisms involving knowledge of the design space:** These strategies involve guided exploration using knowledge of characteristics of design space to improve convergence towards final solution. Examples of such techniques include, but are not limited to, Fuzzy Logic, Markov Decision Process (MDP) [1,23], Genetic [24,25] and Evolutionary Algorithms [26,27]. The fuzzy logic based DSE presented in this paper can be classified into this category. However in order to compare a wider range of techniques with the presented one an overview of other classes of DSE are also discussed as follows.

Exhaustive search mechanisms thoroughly investigate the design space by exploring all the possible configurations. Baghdadi et al. [15] present a DSE technique based on high-level simulation to evaluate the dynamic behaviors of system configurations of a complex architecture. However, due to the higher level of simulation, timing information is not accounted for. Hence additionally, a back-annotation approach based on the RTL (Register Transfer Level) analysis of some implementations allows to extract timing elements needed for performance estimation of all feasible implementations.

Another example of exhaustive search is applied by Monchiero [28] where a target architecture of a configurable number of cores, L2 Cache size, and processor issue width, is analyzed on the basis of power consumption, throughput, and thermal effects. Based on this analysis, further evaluations were performed using various chip floorplans to minimize and study chip temperature effects.

As mentioned above, the random search based schemes provide a viable alternative to typical exhaustive search mechanisms for large design spaces. Bruni et al. [18] present an unsupervised Monte Carlo based design space exploration scheme. In general, the main characteristic of Monte Carlo methods is the use of random sampling techniques to come up with a solution of the target problem. The random sampling technique has been shown to be one of the best techniques to avoid falling into local minima [29].

Another Monte Carlo search based approach for DSE is the use of Simulated Annealing [19,20]. In Simulated Annealing, a new configuration is formed at each iteration by random displacement. If the cost function of this new configuration is less than the previous one, the change is accepted unconditionally; if not, then it is probabilistically analyzed for further exploration [29].

Kreutz et al. [21] present a Tabu search based DSE scheme. The authors propose an optimization algorithm based on the analysis of Network-on-Chip (NoC) topologies and router architectures to find a trade-off between latency and energy constraints. The key concept behind the Tabu search mechanism is a Tabu list that contains moves that are not allowed or prohibitive, and typically includes the recently visited configurations.

Design exploration based on random search techniques such as Monte Carlo, Simulated Annealing and Tabu Search are robust and the literature reviewed suggest their usefulness in general. However, typically these techniques are applied as an off-line process, and require to collect sufficient statistical information before actually starting the design process.

In contrast to exhaustive search and random search schemes, heuristic exploration based techniques involve knowledge of the design space in the search process. One such example of work is presented by Beltrame et al. [1] that employs Markov Decision Processes (MDP). MDP is a reinforcement learning method in which design states are explored in a decision tree probabilistically according to values that have been learned over time. For initial estimates this search typically produces sub-optimal results. However, over a number of trials, the MDP can be trained to produce high-quality architectures [30]. Beltrame et al. [1] have applied MDP to derive custom Very Long Instruction Width (VLIW) processors for various image and video compression algorithms. The authors have adopted a unique approach based on automated guided search by estimating the impact of varying architectural parameters probabilistically and performing simulations only when the estimates are insufficient. Consequently, the number of expensive simulations is reduced. However, this approach requires the availability of an appropriate estimation methodology, which is not generally present in case of arbitrary Chip Multiprocessor (CMP) architectures [31].

Kang et al. [24] present a DSE framework called Magellan. The proposed framework applies a machine-learning approach for the design space optimization problem, by iterative benchmarks simulations on available processor cores. Their work contain a comparison of single objective algorithms such as (genetic algorithms, ant