Microprocessors and Microsystems 37 (2013) 649–660

Contents lists available at SciVerse ScienceDirect

Microprocessors and Microsystems

journal homepage: www.elsevier.com/locate/micpro

Design of a novel differential on-chip wave-pipelined serial interconnect with surfing

M. Bhaskar *, A. Jaswanth, B. Venkataramani

Department of Electronics and Communication Engineering, National Institute of Technology, Tiruchirappalli, India

ARTICLE INFO

Article history:
Available online 25 June 2013

Keywords:
Differential serial interconnect
Logical effort
Repeater insertion
Surfing
Wave-pipeline

ABSTRACT

In the literature, surfing technique has been proposed for single ended wave-pipelined serial interconnects to increase the data transfer rate. This uses uniform repeaters (UR). In this paper, two novel surfing techniques, one using uniform repeaters (UR) and another using non-uniform repeaters (NUR) are proposed for differential wave-pipelined serial interconnects. The method of logical effort is also proposed for the design of both UR and NUR. To evaluate the efficiency of these techniques, 40 mm metal 4 interconnects using the proposed surfing techniques are implemented along with transmitter, receiver and delay locked loop(DLL) in UMC 180 nm technology and their performances are studied through post layout simulations. From this study, it is observed that the differential surfing technique using UR and NUR achieve 3.0 times and 4.15 times higher data rates respectively compared to the single ended scheme whose maximum data rate is 1.33 GB/s.

1. Introduction

As the CMOS technology scales down, transistor sizes get reduced and this in turn increases the speed of the logic blocks [1]. The interconnects between the transistors, referred to as local interconnects, become shorter as technology scales down. However, interconnects used for routing signals between logic blocks, known as global interconnects, do not scale in length from one technology to another [2] and they limit the maximum data rate for on-chip communication. In order to achieve high data transfer rates in circuits using deep submicron technologies, the delay through the global interconnects needs to be reduced. For this purpose techniques such as repeater insertion [3], wire sizing [4], low swing signalling [5] and pulsed wave interconnects [9,10] have been proposed in literature. However, even with these techniques, the time required to transmit data across chip may be several clock periods or handshake cycles.

An overview of the techniques used for interconnects in SoC design is presented next. Delay of interconnect is reported to be proportional to the square of length in [1]. Repeater insertion technique proposed in [3] makes the delay of RC interconnect line to be a linear function of length. The expressions for obtaining the optimum number of repeaters and their size for minimizing the delay of RC interconnects have been reported in [3]. For an interconnect modelled as an RC network, width is considered as a design parameter and it is shown that the repeater insertion outperforms the wire sizing [4]. It is reported in [6] that the delay can be decreased by maximizing the line inductance particularly in low resistance materials with fast signal transitions. In [7], it is shown that the delay of on-chip interconnect obtained using RLC model is less compared to that using RC line model. However, the repeater insertion technique results in larger area, higher complexity in placement and routing and higher power dissipation. To overcome this, the repeater-less interconnect is proposed in [8]. It uses phase shift keying signalling scheme. This maximizes the inductive behaviour and achieves almost near speed of light latency in silicon dioxide with high data rate on-chip interconnects.

The pulsed wave interconnect is proposed for global interconnects in SoC applications in [9,10], where sharp current pulses are used to maximize the inductive behaviour. The pulsed current-mode signalling scheme is proposed in [10] for near speed of light on-chip communication. This uses output multiplexing scheme at the transmitter. As it requires a driver for each input to be multiplexed, it results in more area and power dissipation. To overcome this, the input multiplexed voltage mode transmitter using pseudo NMOS logic is proposed in [11] and it requires only one driver for all the inputs. However, this architecture uses ratioed logic and sensing logic zero level at higher frequencies becomes difficult.

For single ended serial interconnect, an alternate technique known as wave-pipelining is applied to conventional repeater insertion technique to replace the global clocks with local clocks in [12]. Wave-pipelining enables multiple data waves to propagate through an uniformly buffered global interconnect allowing to transmit data at a higher rate. However, the data sent through

* Corresponding author.
E-mail address: bhaskar@nitt.edu (M. Bhaskar).

0141-9331/$ - see front matter © 2013 Elsevier B.V. All rights reserved.
http://dx.doi.org/10.1016/j.micpro.2013.06.002

wave-pipelined interconnects are not reliable. To overcome this problem, surfing technique is proposed in [13] for single ended interconnect. In this technique, a control signal denoted as 'req' is transmitted in a separate line along with each buffered wave-pipelined interconnect segment. This generates the surfing signal 'fast' that controls the propagation delay of each segment. When 'fast' is true, the delay of the buffer in the particular interconnect segment becomes lesser than the normal value. The circuit used in [13] to generate signal 'fast' from 'req' needs a setup timing constraint of about one fourth of the clock period. The reliability of data transmitted is ensured by the 'req' signal but reliability of the transmission of 'req' is not ensured.

In [14], a differential wave-pipelined serial interconnect is proposed to overcome the constraints in single ended scheme. In this technique, the complementary signal path is used to surf the true signal path and vice versa. A separate line is not required to propagate the control signal. It eliminates the setup time constraint and the data reliability is ensured both for true and complement signals. The surfing scheme proposed in [14] is capable of surfing only one signal path (either true or complementary) at a time i.e. when the complementary signal is delayed with respect to the true signal, the surfing signals generated speeds up only the complementary signal path and vice versa.

In this paper, for differential wave-pipelined interconnects, a novel surfing technique which generates the surfing signals during the overlapping period of the true and complementary paths is proposed. This surfs both the true and complement lines at the same time till they are exactly complement to each other. Thus it provides a higher data rate through the differential serial interconnect as compared to [14].

The proposed surfing scheme is also implemented for differential wave-pipelined interconnects with non-uniformly buffered interconnect segments where the length of the interconnect segment and the size of the buffer driving the segment increases progressively. For the purpose of comparison, differential wave pipelined serial interconnect using surfing either with uniform or non-uniform repeaters and the transceivers are designed and studied.

The method of logical effort is proposed in [15] in order to design a CMOS circuit such that it operates at a particular frequency consuming the least area and power. The transceivers for interconnects have not been designed using method of logical effort so far. In this paper, the proposed circuits are designed using the method of logical effort for the first time.

The paper is organized as follows: Sections 2 and 3 describe the design of differential wave-pipelined serial interconnect with surfing using UR and NUR respectively. In Section 4, the details of the test chip design for serial interconnect with UR and NUR are presented. Section 5 provides the post layout simulation results and the observations. The concluding remarks are given in Section 6.

2. Design of differential wave-pipelined serial interconnect with surfing and UR

The schematic diagram of surfing circuit proposed for the wave-pipelined differential serial interconnect with UR is shown in Fig. 1. It has true and complementary data wires connected between transmitter and receiver. These two interconnect wires are divided into '*n*' equal segments and uniform size buffers are inserted between each segment along with its control circuitry for surfing. The data transmission will be robust if both true and complementary data are received by the receiver simultaneously.

A modified pair of buffers called the "Controllable Inverter pair" is proposed in this paper to ensure surfing along both true and complementary wires at the same time. The controllable inverter

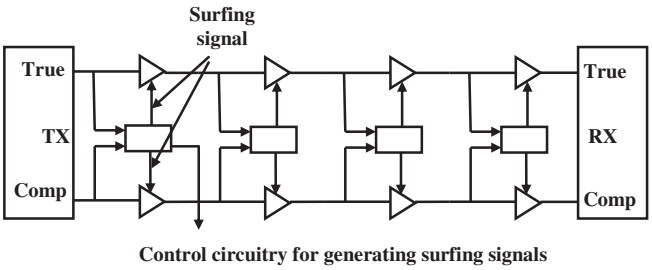

Fig. 1. Schematic diagram of differential wave-pipelined serial interconnect with surfing and UR.

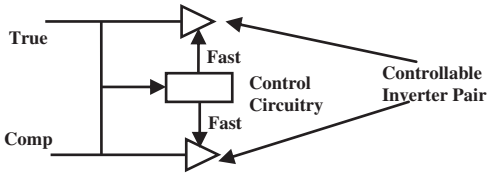

Fig. 2. Block diagram of wave-pipelined segment with surfing.

pair can vary the delay of the buffers when the control signals are activated, so that transmission rate can be made faster or slower i.e. the delay of the data lines can be varied whenever required.

In the proposed scheme, each surfing segment of the wave-pipelined serial interconnect contains a controllable inverter pair, its control circuitry and an interconnect wire. The block diagram of a segment used for surfing is shown in Fig. 2. The timing constraints proposed in [13] for surfing the single ended interconnect is extended for the differential interconnect and the control circuitry proposed in this paper ensures that the surfing pulses are produced inaccordance with the timing constraint given by (1).

$$\delta_{True}^{fast,\max} \leqslant \delta_{Comp}^{slow,\min} \geqslant \delta_{Comp}^{fast,\max} \leqslant \delta_{True}^{slow,\min} \quad (1)$$

where $\delta_{True}^{fast,\max}$ and $\delta_{Comp}^{fast,\max}$ denote the maximum delay of the true and complementary data paths when 'fast' is asserted respectively. $\delta_{Comp}^{slow,\min}$ and $\delta_{True}^{slow,\min}$ denote the minimum delay of the true and complementary data paths when 'slow' (complement of true) is asserted respectively.

These constraints ensure that events in the True and Complementary data paths propagate together at the same speed. It is to be noted that in the proposed scheme, the surfing pulses are produced only when there is reliability issue in the transmission path, whereas in [13], the fast pulses are produced irrespective of the situation.

2.1. Controllable inverter pair

The circuit diagram of the "Controllable inverter pair" is given in Fig. 3. The controllable inverter pair circuit proposed in this paper has symmetrical structure both for true and complement signal paths but it is not so in [14]. This enables the surfing of both true and complement paths at the same time. In Fig. 3 CIN, COUT, TIN and TOUT denote the complementary input, complementary output, true input and true outputs respectively. One pair of inverters is used for true line (TIN) and another pair for the complementary line (CIN). In [14], the delay of the inverter pairs is controlled by the normal surfing signals F1 and F2, whereas, in this paper, it is controlled by both normal surfing signals F1 and F2 and their complement signals F1C and F2C. These two inverters must always be used as a pair because the control signals for surfing these pairs are