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Analytical performance modeling of de Bruijn inspired mesh-based network-on-chips

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ABSTRACT

This paper proposes and evaluates a de Bruijn inspired topology as an efficient alternative to the popular mesh topology for Network-on-Chips (NoCs). The proposed topology (1) provides logarithmic diameter for NoC, (2) offers better performance under uniform, hotspot, and matrix transpose traffic patterns and, (3) consumes lower energy for packet delivery, however, the proposed topology imposes the cost nearly equal to the mesh topology. In addition to the proposed topology, an analytical performance model is proposed in the paper to accelerate the evaluation process of the proposed topology. The model considers a network of M/G/1 queues and accurately estimates the average message latency as a widely used representative for the network performance. Results obtained from the analytical model are in good agreement with those of simulations for a wide range of working conditions such as various network sizes, different message lengths, and different traffic patterns.

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1. Introduction

With recent advances in VLSI technologies, modern chips can accommodate a large number of processing cores as a multi-core chip. Such multicore chips require an efficient communication architecture to provide a high performance connection between the cores. Network-on-Chip (NoC) has been recently proposed as a scalable communication architecture for multicore chips [1]. In NoC paradigm, every core communicates with other cores using on-chip channels and an on-chip router. The on-chip channels construct a predefined structure called topology. Since the network topology has a direct impact on important NoC parameters, e.g., network diameter, bisection width and the routing algorithm, several topologies have been proposed in the literature such as mesh topology [2], hypercube topology [3], tree topology [4], and de Bruijn topology. Each of these topologies has its pros and cons; for example, mesh topology is used in the fabrication of several NoCs because of its simple VLSI implementation, however, other topologies are also favored by NoC designers due to their exclusive features. The de Bruijn topology is one of those topologies that provide a very low diameter in comparison with the mesh topology, however imposes a cost equal to a linear array topology. The de Bruijn topology is a well-known structure which is initially proposed [5] for parallel processing networks. Several researchers have studied topological properties [6], routing algorithms [7,8], VLSI layout efficiency [6] and other aspects of the de Bruijn networks [9]. NoC designers also favor to the de Bruijn topology, since it provides logarithmic diameter and costs equal to a linear array topology [9].

Considering the reputation of the mesh topology and the low network diameter of de Bruijn topology, this paper proposes, evaluates, and models a de Bruijn inspired mesh-based topology for NoCs. The contribution of this paper is threefold. (1) A de Bruijn inspired mesh-based (DIMB) topology for NoCs. In the DIMB topology, each row and column of an $n \times n$ mesh topology is replaced by a de Bruijn topology. Results show that DIMB topology can outperform its equivalent mesh topology in terms of network performance and energy dissipation. (2) A deadlock free routing algorithm has been developed for the proposed topology. This routing algorithm is based on the use of different classes of virtual channels to prevent deadlock situations in the network. The proposed routing algorithm is presented and evaluated in the current study. (3) This paper also introduces the first analytical model to predict the average message latency as a major performance measure in DIMB networks. Analytical models are used by several researchers and designers to achieve significant speed up in the performance evaluations. The proposed analytical model provides a minimum speed up of 400% in comparison with simulation based evaluations.

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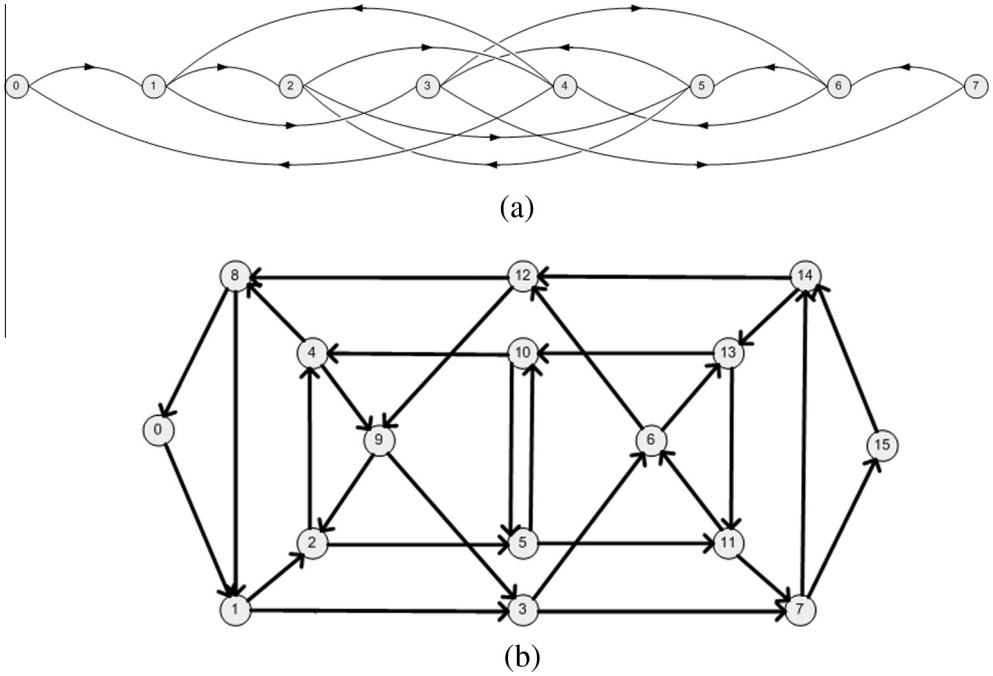

Fig. 1. The de Bruijn network with (a) $N = 2^3$ and (b) $N = 2^4$ nodes.

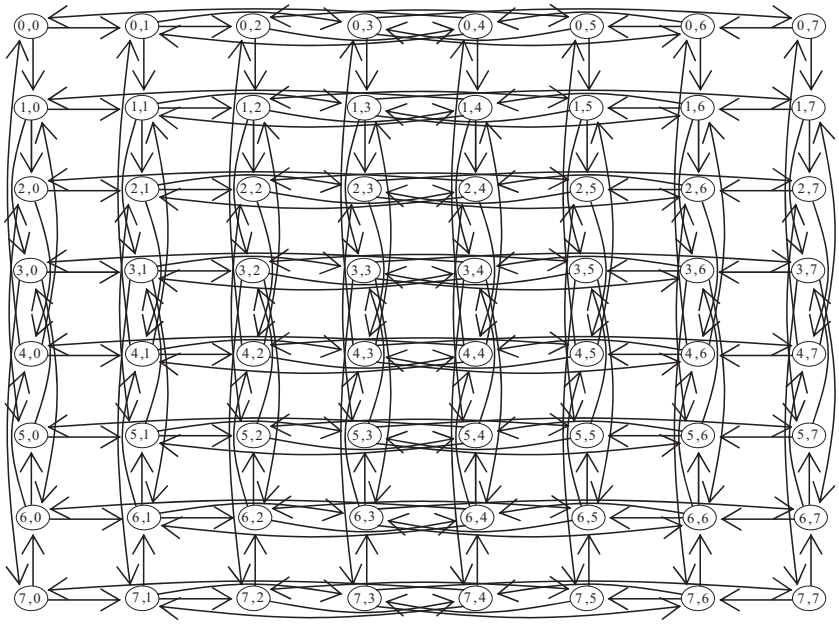

Fig. 2. A DIMB with 64 nodes composed from eight 8-node de Bruijn networks (as shown in Fig. 1a) along each dimension.

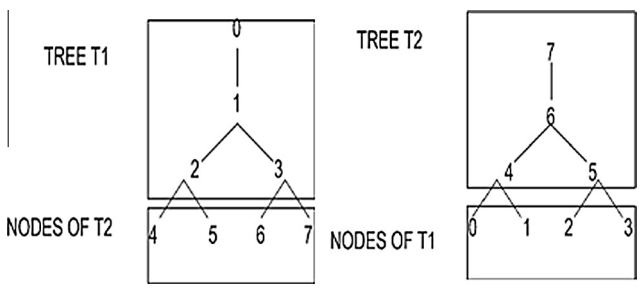

Fig. 3. Trees T1 and T2 for $N = 8$.

The rest of the paper is organized as follows. Section 2 introduces DIMB and Section 3 describes routing algorithm. Section 4 describes the simulation environment and results. Section 5 describes the analytical model and then the model results are validated with simulation results. Finally, Section 6 concludes the paper.

2. The proposed network topology: DIMB

Since the proposed network topology is based on de Bruijn, this section briefly introduces the de Bruijn topology [10,11]. An n-dimensional de Bruijn topology is a directed graph including

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