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Performance evaluation of the augmented data vortex switch fabric: An all-optical packet switched interconnection network

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Abstract

Modern high-performance computing systems require networks with high capacity, extremely high throughput and low latency in order to pass messages between thousands of processors and memory elements. Optical Interconnection Networks (OIN) offer a potentially viable solution to this requirement. An all-optical packet switched interconnection network called a Data Vortex (DV) switch has already been proposed by Yang et al. for the purpose of large scale photonic interconnections. For any interconnection network, fault tolerance and reliability are crucial issues, evaluation of which lacked attention for the case of the DV switch. In our earlier work we therefore presented the results for fault tolerance and reliability analysis of the primary DV switch. We also proposed a new *Augmented Data Vortex (ADV) switch* fabric, to improve the fault tolerance of the primary DV switch. The performance as regards fault tolerance of the ADV switch was computed and detailed results were obtained. In this paper, performance of ADV is investigated with reference to parameters such as latency and injection ratio (throughput) by means of numerical simulations. A uniform random traffic model has been used for the performance evaluation. The results obtained are compared with the results reported for the DV switch. The results show that the ADV switch with enhanced fault tolerance also improves the performance regarding latency. For same switch sizes (i.e. the same number of angles A, and height H) the injection ratios (throughput) for the DV and the ADV switches are comparable. Hence it can serve as a suitable candidate for high performance computing.

Keywords: Optical Multistage Interconnection Networks (OMINS); Network fault tolerance; Data vortex; Augmented data vortex; Throughput; Latency

1. Introduction

Modern high-performance computing systems require networks with high capacity, extremely high throughput and low latency in order to pass messages between thousands of processors and memory elements [1]. Optical Interconnection Networks (OIN) offer a potentially viable solution to this requirement as fiber-optic components are capable of carrying many terabits per second of encoded optical data when full Wavelength Division Multiplexing (WDM) is used, while maintaining near speed-of-light limited transit latencies [2,3]. An all-optical packet switched interconnection network, called a Data Vortex (DV) switch, has already been proposed by Yang et al. [4–8] for the purpose of large scale photonic interconnections, and

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satisfies the requirements of high throughput and low latencies, maintaining operation in an all-optical domain and thus eliminating the limitations caused by electronic communications bottlenecks.

Since the interconnection networks are at the heart of the system in high performance computing and supercomputing applications, their fault tolerance and reliability are unavoidable issues. But this fundamental issue, namely the fault tolerance and reliability analysis of the DV switch, lacked attention. In our earlier work we therefore presented the results of fault tolerance and reliability analysis of the primary DV switch [9]. Although in the DV switch there are multiple paths between each source–destination pair, and thus it is inherently fault tolerant; since each node is a 2 input–2 output (2×2) switching node, each node is single-fault tolerant. Only one of the two output links of the node can be allowed to fail. Failure of both the output links of a node may cause disconnectivity among certain source–destination pairs.

We proposed a new *Augmented Data Vortex (ADV) switch* fabric [10], which incorporated all the advantageous features of the DV switch and also improved the fault tolerance of the primary DV switch. A new self-routing scheme and a priority scheme for distributed control signaling in the switch were described. The network utilizes the augmented links in addition to the already existing links in the primary switch [4] to route the packet when the faults occur. The ADV switch provides more alternate paths than the primary switch while the routing algorithm is much simpler. A multiplexing scheme at input ports and output ports was proposed for enhanced fault tolerance. Computation of the reliability and fault tolerance of the new architecture via an analytic model was shown. Finally, we compared the ADV switch architecture with the primary architecture, DV, with respect to fault tolerance and reliability [10].

In this paper we present the performance evaluation of the ADV switch with reference to parameters such as latency and throughput (injection ratio), using numerical simulations. As will be seen through our results, the ADV switch, which has basically been proposed as an all-optical packet switched interconnection network with enhanced fault tolerance, also exhibits much lower latencies than and comparable throughput to the DV switch. Thus it can serve as a suitable candidate for high performance computing and supercomputing applications, in which fault tolerance and latency are important issues.

In Sections 2–4 we present an overview of the ADV switch [10], for the purpose of clarity and understanding. In Section 2, we present the 3-dimensional switch model, the labeling and numbering scheme, and interconnection of the nodes for the ADV switch. A priority scheme for distributed control signaling in the ADV switch is also explained here. In Section 3 we propose the conversion of the 3-dimensional switch to an equivalent planar model, which is more suited to an explanation of routing, analysis for fault tolerance, and comparison with other chained MINs. In Section 4, the routing procedure for the ADV architecture is presented. In Section 5, the performance of the ADV is investigated with reference to parameters such as latency, and injection ratio (throughput), by means of numerical simulations. A uniform random traffic model has been used for transmission of packets. The results are compared with those of the DV switch. In Section 6 we give the conclusions and discussions.

2. Labeling, numbering, interconnection of nodes, and distributed control signaling in ADV switch

The ADV switch proposes two improvements over the primary DV switch. (1) It uses a 3 input–3 output node, represented as a 3×3 node (excluding the control inputs and outputs at each node), as compared with the 2 input–2 output node (2×2) node used in the primary DV switch [4]. This increases the number of multiple paths between any source–destination pair and hence improves fault tolerance. (2) Multiplexing at input ports and output ports is proposed which further enhances the fault tolerance in the ADV switch. At present we are not looking into the physical implementation of such a node, since we are only interested in the performance evaluation of the proposed augmented data vortex switch from the point of view of latency and throughput (injection ratio), and its improvement over the primary data vortex switch. In this section we discuss the labeling, numbering, interconnection of nodes, and distributed control signaling in the ADV switch.

2.1. Labeling and numbering scheme

For ease of comparison, we prefer to use the same labeling scheme for nodes as in [4–8]. The topology is arranged as a collection of richly connected 3×3 routing nodes on multiple fiber cylinders. The switch fabric size is characterized by two parameters 'A' and 'H', representing the number of nodes along the 'angle' and 'height' dimensions, respectively. 'A' is typically set to be a small odd number (<10) and is independent of the