Microprocessors and Microsystems 39 (2015) 512–520

Contents lists available at ScienceDirect

Microprocessors and Microsystems

journal homepage: www.elsevier.com/locate/micpro

Designing quantum-dot cellular automata counters with energy consumption analysis

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ARTICLE INFO

Article history:
Available online 6 August 2015

Keywords:
Nanoelectronics
Quantum-dot cellular automata (QCA)
Memory
Counter
Energy consumption

ABSTRACT

Quantum-dot cellular automata (QCA) exhibits a new paradigm at nanoscale for possible substitution of conventional CMOS technology. Most of the research works in QCA domain have completely ignored the significance of energy consumption constraint in designing circuits. In this study a low complexity and energy-efficient QCA *T* flip–flip as well as high-performance single-layer synchronous counters are proposed. By cascading the proposed *T* flip-flop and a suitable level converter, a QCA-compatible structure for falling edge triggered *T* flip-flop is achieved. This circuit functions as the chief element for constructing synchronous counters. QCADesigner and QCAPro tools are used for evaluating the functionality and calculating dissipated energy of the circuits, respectively. Results indicate the superiority of the proposed circuits in terms of complexity, latency and energy consumption as compared to their state-of-the-art counterparts. The proposed *T* flip-flop demonstrates 18% leakage energy improvement besides the considerable value of 56% switching energy improvement in 0.5Ek tunneling energy level as compared to the best ones. It is worth mentioning that 41%, 44% and 45% optimizations in the number of cells in addition to 15%, 25% and 33% optimizations in the area are achieved for the proposed mod 4, mod 8 and mod 16 counters, respectively, in comparison with the best previous results.

1. Introduction

One of the hottest issues in today's nanoelectronics is quantum-dot cellular automata (QCA) which was firstly introduced by Lent et al. in 1993 [1]. In this paradigm, interfering of quantum physics and nanotechnology in electronics manufacturing leads to smaller and more efficient circuits [2]. The logic of quantum-dot cellular automata is very similar to the binary logic models commonly used in computer architecture [3,4]. Attractive features of this new technology such as high speed, low power consumption [5,6] and straightforward designing rules [3,7] have resulted in many research works in last decade.

One of the most attractive areas in QCA technology is designing memory cells [8]. Saving data in computer architectures is a vital notion and consequently memory cell is among the most momentous and fundamental building blocks in digital systems which contribute to the major part of the area, delay and power consumption on electronic chips [9,10]. As a result, any optimization in its complexity and performance directly improves the performance of whole system.

To date, lots of studies have been carried out by the researchers in designing efficient QCA memory cells, such as different structures for random access memory cell [10,11,15], well-optimized QCA architectures for flip-flops [13–18] and counter designs [12,13]. In addition, logical and arithmetical circuit designs have been extensively investigated in several studies [20–24,28,29].

It is worth pointing out that all the mentioned studies have completely dropped the importance of energy consumption in QCA architectures. The first accurate QCA power dissipation model among numerous performed studies has been proposed by Timler and Lent [4]. According to the valuable results of this study, Srivastava et al. [5] have proposed an upper bound power dissipation for QCA circuits. In 2011, QCA Pro tool was developed as an accurate power estimation tool based on the model presented in [5] by capability of presenting total energy consumption using two core terms called "leakage energy" and "switching energy" [6].

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http://dx.doi.org/10.1016/j.micpro.2015.07.011
0141-9331/

The main target in this research is to propose low-complexity and energy-efficient memory structures. Therefore, first, an innovative design and implementation for QCA *T* flip-flop is proposed. Afterwards, by integrating the proposed well-optimized and energy-efficient *T* flip-flop as the fundamental element, different counter circuits (up to 4-bit) are designed.

The rest of the paper is organized as follow: an introduction to QCA preliminaries and a review on QCA counter structures are provided in Sections 2 and 3, respectively. The proposed design for QCA *T* flip-flop and related structural and energy consumption analyses are addressed in Section 4. The discussion over the proposed synchronous counter and its performance evaluation are presented in Section 5. Finally Section 6 concludes this study.

2. QCA background

2.1. Fundamental structures

The QCA stores logic states not as voltage levels but rather based on the position of individual electrons [1]. As shown in Fig. 1a, the QCA cell contains four quantum-dots that are located at the corners of a square. There are two additional mobile electrons for a cell which are allowed to tunnel among neighboring sites. The existing columbic repulsion between two electrons forces them to locate in opposite corners pinpointing the concept of polarization (Eq. (1)). Consequently, there are only two stable states for representing the binary information "1" and "0" [2].

The QCA standard wire can be simply constructed by cascading a chain of QCA cells as illustrated in Fig. 1b. In addition, a QCA inverter chain is constructed using 45° rotated QCA cells [3].

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{\rho_1 + \rho_2 + \rho_3 + \rho_4} \quad (1)$$

The fundamental QCA elements are inverter and majority gates. To reverse the QCA cell's polarization, inverter is used as illustrated in Fig. 2a. Three-input majority gate can be designed by five QCA cells set in a cross. As shown in Fig. 2b, cells *A*, *B*, and *C* are input cells and cell *M* is the output cell that is polarized according to the majority of input cell polarizations. The logic function of the 3-input majority gate can be expressed by Eq. (2). Logical 2-input AND and OR functions can be implemented using 3-input majority gate by setting one arbitrary input cell to binary '0' and '1', respectively [3].

$$M(A, B, C) = AB + BC + AC \quad (2)$$

The rewarding achievement of implementing a 3-input majority gate with only 5 QCA cells motivated the researchers to theorize an innovative structure for 5-input majority gate. First attempt has been made in [21] by Rahimi Azghadi et al. leading to a three-dimensional realization of 5-input majority gate. This design which is shown in Fig. 2c proved the fundamental concept of this gate. Afterward, the authors of [23] have implemented a single layer 5-input majority gate using 10 QCA cells in a specific cell arrangement which is illustrated in Fig. 2d. The logic function of the 5-input majority gate can be expressed by Eq. (3).

$$M(A, B, C, D, E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE \quad (3)$$

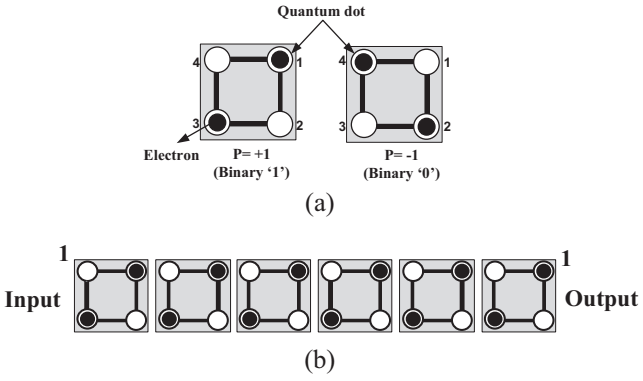

Fig. 1. QCA basic cell and two possible polarizations (Fig. 1a), QCA wire (Fig. 1b).

2.2. Clocking mechanism

Although clock signals in CMOS circuits are exclusively applied for synchronization of flip flops, they are considered to supply the power gain for the cells and to control the data flow in QCA circuits. QCA clocking is introduced with four different and successive phases, so QCA circuits are categorized into four clock zones where the cells in a particular zone receive same clock signal. As illustrated in Fig. 3, four clock phases are: switch, hold, release, and relax. A 90° phase-delay exists between the subsequent clock zones [7,10].

As is described in [3], in a robust 3-input majority gate structure for omitting the noise effects, the input wire cells should be positioned in the first clock zone, the middle QCA cells should be positioned in the second clock zone with the output wire positioned in the third clock zone.

2.3. Implementation issues

There are four dissimilar techniques for single layer implementation of quantum-dot cellular automata as is thoroughly described in [25] (molecular, metal-island, semiconductor, and magnetic). If the fabrication problems could be efficiently solved all indications are physically feasible. One of the most controversial hurdles in practical QCA circuits is their operational temperature (below 7 K [26]). This extremely low temperature is considered for properly distinguishing of a QCA cell states (the ground state and the first excited state) [24]. Specific studies also have been fulfilled for inspecting the likelihood of increasing QCA temperature [27]. These works show that in order to provide QCA circuits with higher temperatures, the physical features of the QCA cells need to be changed. This issue can be triumphed by different approaches such as: optimizing the distance between cells and arrangement of 3D QCA. It is noteworthy that experimental illustrations of primary gates in magnetic QCA are accomplished in [30]. As is clearly described in [24,25], multilayer QCA circuits are prone to numerous defects and cannot be implemented with ongoing technologies. Therefore, much attentions should be paid to designing single layer QCA circuits.

3. A review on QCA counter architecture

The main structural components for designing sequential circuits are flip-flops [14]. Although the inherent capability of QCA technology makes each QCA cell a single D latch controlled by the clocking circuitry, it is important to design QCA flip-flops controlled by an enabling mechanism (independent of QCA clocking) such as conventional CMOS. Memory concept in QCA loop-based approach is realized by a loop containing four clock zones. As illustrated in Fig. 4, this element can be used for storing one bit data during one clock cycle employing feedback mechanism.

In order to implement a high performance synchronous counter in QCA, designing well-optimized and high speed edge triggered flip-flops is the first vital issue. The authors of [8] have made an