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# Fault tolerant routing algorithm based on the artificial potential field model in Network-on-Chip

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ABSTRACT

Recent advances in semiconductor technology enable the VLSI chips to integrate hundreds of intellectual properties with complex functionality. However, as the chip scales, the probability of faults is increasing, making fault tolerance a key concern in designing the large scale chips. The fault tolerant routing algorithms can guarantee sustained communication even the faults exist. It is an efficient technique to achieve fault tolerance in Networks-on-Chip. In this paper, we propose a new model based on the theory of artificial potential field (APF) to design various fault tolerant routing algorithms. In our model, the faults are considered as the poles of the repulsive potential fields while the destinations as the poles of the attractive potential fields. Messages are attracted to destinations and repelled by faults in the combined artificial potential field. The parameters used in the proposed APF based model are optimized through theoretical analysis and simulation experiments. They can support flexible fault tolerant routing algorithms. Finally, we evaluate the performance of the proposed fault tolerant routing algorithm based on the APF model in 2D-mesh NoCs with random faults. The simulation results show that the proposed APF based model is feasible and the routing algorithm can maintain good network performance.



## 1. Introduction

Networks-on-Chip (NoCs) are promising to overcome the limitations of the traditional on chip communications, such as poor scalability, limited bandwidth and high power consumption, etc. As the integration technology advancing, silicon features approach the atomic scale. Hundreds of heterogeneous integrated modules can be interconnected via NoCs [1]. However, the reduced feature sizes make on-chip communications more difficult [2]. The increasing wire delays, cross-talk noise and device wear-out all pose great threats on NoC reliability. These effects can result in the failures of transistors and wires. Thus, on-chip circuits are becoming vulnerable to transient, intermittent and permanent errors [3]. The permanent failures due to material aging, electromigration, or mechanical or thermal stress can incapacitate a processing or storage core or a communication link, especially for a router in the NoCs which will make the communications crash down [4,5]. Although NoCs do not inherently support fault tolerance, they provide chances to design various fault tolerant mechanisms due to the good path diversity. The fault tolerant routing algorithms are able to ensure the messages routing around faulty nodes or links. Thus, they can make the NoCs reliable.

Various fault tolerant routing algorithms are proposed in the literature. The stochastic routing algorithms use flooding scheme including probabilistic flooding and directed flooding [6]. These algorithms demonstrate a high message arrival probability [7]. But they require high power consumption for the abundant of redundant messages transmitted in the network. The multiple paths routing methods can achieve fault tolerance by using multiple routing paths for the messages

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[8]. However, the packets of the same message may arrive at the destination out of order. The in-order delivery results in high complexity of the router architecture. Misrouting make the messages take alternate paths around the faulty nodes [9–11]. These mechanisms are based on the rectangular or convex fault regions models which make the potential fault free nodes disabled. In addition, the unbalanced traffic load around the fault regions may result in serious congestion, and the using of virtual channels or turn models to avoid deadlocks also bring extra costs. Some methods based on graph theory are also used to analyze the fault tolerant problems [12–16]. In [14], the t/k-diagnosis strategy is used to analyze the degree of diagnosability of the so-called BC graphs, and the diagnosability of the DCC (disjoint consecutive cycles) linear congruential graph G (F,n) is studied in [16]. The node faults are addressed in an injured n-cube network [15].

In this paper, we proposed an artificial potential field (*APF*) based model to design fault tolerant routing algorithms in NoCs. The model supposes two artificial potential fields in NoCs. The repulsive potential fields are generated at the faulty nodes while the attractive potential fields are generated at the destination nodes. Messages are attracted to the destinations and repelled by faults in the *combined artificial potential field*. Thus, the messages choose routing paths according to the input artificial forces. The key issue of the *APF* based model is to find efficient potential functions. Inspired by the natural electrostatic potential fields, we design the potential functions of the attractive and repulsive artificial potential fields. The proposed *APF* based model is implemented with limited global fault information. The simulation experiments are conducted to analyze the effect factors of the *APF* based model. We can optimize the parameters used in the *APF* based model through these experiments. Finally, we evaluate the performance of the *APF* based model in 2D-mesh NoCs with random faulty nodes. The end to end (ETE) delay and the throughput derived from the simulation demonstrate that the proposed *APF* based model is efficient to obtain fault tolerance in NoCs.

The rest of this paper is organized as follows. Section 2 gives the definition of the proposed *APF* based model. The fault tolerant routing algorithms based on the proposed model are discussed in Section 3. In Section 4, we implemented some experiments to analyze the parameters used in the model. Then the performance of the routing algorithm is evaluated through OPNET. Finally, we draw some conclusions in Section 5.

## 2. Artificial potential field based model

The faults occurred in NoCs may lead to the crashing down of the whole system, such as the faulty nodes may prevent some messages routing to their destinations. The failed nodes are obstacles when the messages move in NoCs. We develop a new method based on the artificial potential field to solve the problems caused by the permanent failures in a Network-on-Chip. The faulty nodes are considered as the poles of repulsive potential field, and the destinations as the poles of attractive potential field. Thus, the force of the *combined artificial potential field* will drive the messages to its destinations while bypassing the faulty nodes. Fig. 1 shows an example of an artificial potential field in a $9 \times 9$ 2D-mesh NoC. Node (2,4) and node (4,4) are assumed to be the faulty node and the destination node respectively.

In such a *combined artificial potential field*, the position of the destination node should be the location of the lowest potential. On the contrary, the position of the highest potential is located in the neighborhood of the faulty node. A message is routed to the destination node along the decreasing potential path. It tries to avoid choosing the increasing potential path which leads to the faulty nodes. Thus, the messages will move from a high potential position to a low potential position in the negative gradient direction.

Let $D(x_d, y_d)$ represents the destination node, and $F_1(x_{f_1}, y_{f_1}),\ F_2(x_{f_2}, y_{f_2}), \ldots, F_i(x_{f_i}, y_{f_i})$ and $F_N(x_{f_N}, y_{f_N})$ represent the faulty nodes. $N$ is the number of faulty nodes in the network. Then the potential functions should meet the following equations.

$$U(\mathrm{r})_{N\_D(x_d,y_d)} = \left[U_{\mathrm{G}}(r_1) + \sum_{i=1}^{N} U_{0_\mathrm{i}}(r_{2_i})\right]_{N\_D(x_d,y_d)} = \mathrm{U}_{\min} < 0, \tag{1}$$

$$U(\mathrm{r})_{N\_F(x_{f_i},y_{f_i})} = \left[U_{\mathrm{G}}(r_1) + \sum_{i=1}^{N} U_{0_\mathrm{i}}(r_{2_i})\right]_{N\_F(x_{f_i},y_{f_i})} = U_{\max_\mathrm{i}} > 0,\ 1 \leqslant i \leqslant N, \tag{2}$$

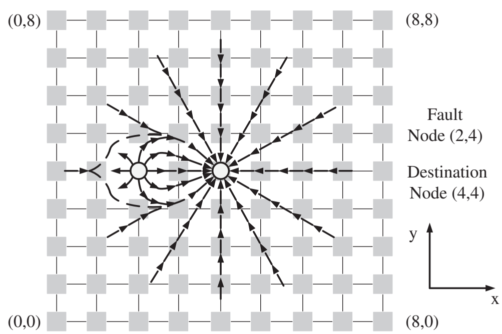


**Fig. 1.** An example of an artificial potential field in a $9 \times 9$ 2D-mesh NoC.