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STorus: A new topology for optical network-on-chip

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ABSTRACT

Optical Network on Chip (ONoC) architecture is emerging as a promising candidate in multiprocessor systems-on-chip (MPSoC) because of ultrahigh communication bandwidth, low latency and power consumption. The topology and layout of ONoC has a great impact on the network performance. Waveguide crossing in the topology would influence power consumption and crosstalk noise, which could influence the size of ONoC directly. In this paper, a screwy torus topology (STorus) and a new optical router are proposed. We divide an optical network into two subnets, and connect them with gateway. The diameter of STorus is half of Torus-based ONoC and almost a quarter of Mesh-based ONoC. To reduce the number of crossing, waveguide hierarchy has been employed. The simulation results show that the new topology can improve throughput by 59.1% compared with traditional mesh under hotspot traffic, and 52.3% compared with traditional mesh under uniform traffic.

1. Introduction

WITH the growth of demand in communications, processing system with high performance is highly needed. Multi-Processor Systems-on-Chip (MPSoC) integrate many processors in a chip, and can dispose huge information [1,2]. The improvement in performance achieved by the use of a multi-core processor depends on not only how efficiently the cores dispose information, but also the efficiency that cores communicate with each other [3,4]. An efficient on-chip communication architecture and network layout can help take full advantage of the computation resources offered by multiply processors. Therefore, on-chip interconnects in the chip multiprocessor gradually change from bus interconnects to networks-on-chip (NoC) [5]. However, with the growth of communication demand, metallic-interconnect-based NOC was challenged because of limited bandwidth, long latency, electromagnetic interference and many other problems.

Optical Network-on-Chip (ONoC) rise with the development of silicon nanophotonics and CMOS-compatible components, and it has generally become the consensus that future on-chip interconnection network should also exploit as many advantages that optics can provide as possible [6–8]. Compared with electrical interconnect, optical interconnect have the advantage of providing low latency, high bandwidth, and energy-efficient communication, which makes ONoC more attractive for future energy-efficient and high-performance on-chip interconnection [9]. Since chip size is limited, ONoC faces with expandability problem. Then Three-Dimensional Integrated Circuit architectures are proposed and it becomes the focus of researchers. Such architecture consists of electrical layers, whose main role is to configure resource, and at least one optical layer stacking upon the electrical layers. It makes possible the realization of mixed-technology eletronic-controlled ONoCs. Based on the three-dimension integration technologies, researchers designed many three-dimension NoC architectures base on three-dimension network topologies to improve performance of NoC [10,11]. In this paper, a new ONoC architecture is proposed, and it employs three-dimension integration technologies, which obtains all the strengths of ONoC and three-dimension integration technologies.

The network topology of ONoC consist of the layout and interconnection relationship of the devices on-chip, for instance, IP cores, optical routers, and waveguides [14]. Taking the mesh topology as an example, all the optical routers are connected via waveguides in a grid shape, and each IP core is connected to a local optical router. It is widely applied because of regular layout and simple architecture [15,16]. However, the mesh topology [34] has a barrier, high diameter, which would result in a high packet hop count. Under this condition, torus topology is employed [17,18]. Through applying long wraparound waveguides, torus can reduce the diameter. However, it is imperfect, because the added waveguides would result in additional waveguide crossings, which aggravate the optical loss. In order to utilize the silicon photonics technology fully, several new architectures were designed. For instance, the 2D-HERT, proposed by Koohi et al. [19], built upon

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clusters of processing cores locally connected by optical rings. Different clusters are interconnected by global optical 2D rings. Le Beux et al. proposed a contention-free new architecture based on optical network on chip, called Optical Ring Network-on-Chip (ORNoC) [20]. In this architecture, a wavelength is reused for multiple communications on a single waveguide, to take into account the design constraints. However, most of these innovative optical architectures are based on traditional mesh and torus, and they still face with loss, diamond and end-to-end delay problems. The new topology proposed in this paper can deal with these problems in some degree.

Compact optical routers are important components for ONoC [21]. Several silicon on-chip optical routers have been proposed [22–24]. Among these optical routers, 5×5 optical routers are widely employed [12,13,25]. Generally, on-chip optical routers are adopted in a 2D network architecture, which would introduce many waveguide crossings, and cause a great power loss as a result. In order to decrease the waveguide crossings and power loss as many as possible, a new optical router is proposed in this paper.

In this paper, we propose a new ONoC topology, Screwy Torus architecture (STorus), which takes advantage of the strengths of ONoC and three-dimension integration technologies. STorus also remits the hop count, diameter, and optical loss problems. Through employing two types screwy ring, a regular architecture turns up. The optical network is divided into two subnets with each subnet consisting of a STorus architecture. With the help of gateway, each IP core is capable of serving two subnets simultaneously. It is proved that STorus is a compact topology because it leads to shorter path and less optical loss. In addition, we design a relevant 5×5 optical router, which is appropriate for Three-Dimension architecture. The routers base on silicon micro-ring resonators (MRs) and hierarchy waveguides. Last but not least, Three-Dimension layout is adopted and part of waveguides are relocated outside the optical network, which result in less waveguide crossing and less optical loss.

2. Screwy torus architecture (STorus)

To exploit the properties of optical interconnect further, STorus architecture (Fig. 1) is designed, which is devised by reconfiguring the connectivity of IP cores and routers, and replacing the waveguides. For a $N \times N$ network, the number of IP core is N^2, gateway is $N^2/2$, and optical router is N^2. In addition, N is even. An 8×8 architecture is shown in Fig. 1. STorus architecture divides one optical network into two subnets. All the optical routers that locate in odd columns of odd lines and even columns of even lines belong to the same subnet, and all the other optical routers that locate in even columns of odd lines and odd columns of even lines belong to the other subnet. For an optical network with size 8×8, as shown in Fig. 1, all the blue nodes situate in one subnet, named subnet 0; and all the green nodes situate the other subnet, named subnet 1. The two IP cores that connected by one gateway belong to two different subnets. The two nodes that connected by one gateway are Upper and lower adjacent. For example, as shown in Fig. 7, the first line node share gateway with its nether node in the second line, and the third lines node share with its nether node in the fourth line. Because one subnet overlaps another after rotating it clockwise by 90 degrees, it is possible to understand the entire network by analyzing one subnet. Here we choose subnet 0. STorus topology is comprised of 5×5 optical routers and a series of interconnection. The interconnection is shown in Fig. 2. Eight nodes that with the same color are connected by a screwy ring. The rings just like number 8, which are shown as blue ring. Eight different color nodes that located in the same diagonal are connected with nodes, which are located in the fourth line below them by a screwy ring. The rings like number 8 also, which are shown as green ring shown in Fig. 2. Each ring includes eight nodes, no matter green rings or blue rings. After moving the subnet 0 topology of STorus in a counterclockwise direction by 45 degrees, and moving up the shaded area, we get a $N \times (N/2)$ logic topology. Nodes that locate in one horizontal rank belong to one horizontal ring, and nodes that locate in column j belong to one vertical ring with nodes that locate in columns $j+N$. As to an 8×8 network, the logic topology is shown as Fig. 3. Waveguide that connects eight horizontal nodes are located in a same layer, which are shown as blue lines in Fig. 3. Waveguide connecting eight vertical nodes locate in another layer which are shown as green lines in Fig. 3.

To make it clear, we establish a coordinate system for STorus topology as shown in Fig. 3. We define the direction from left to right is direction *x* and from up to down is direction *y*. Eight nodes that locate in a vertical ring share the same *x*-coordinate. The left

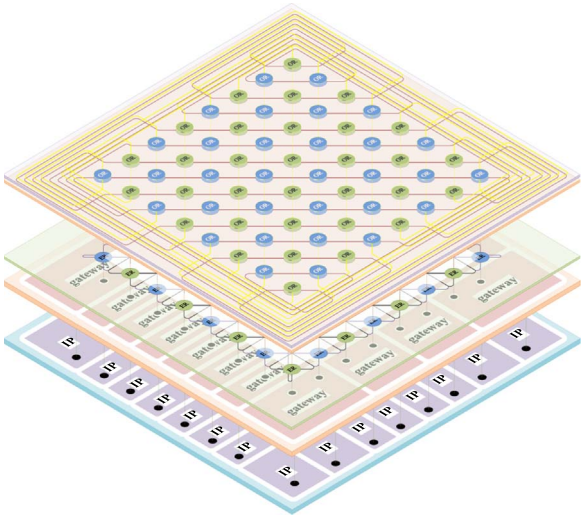

Fig. 1. Logic STorus architecture. (For interpretation of the references to color in this figure, the reader is referred to the web version of this article.)

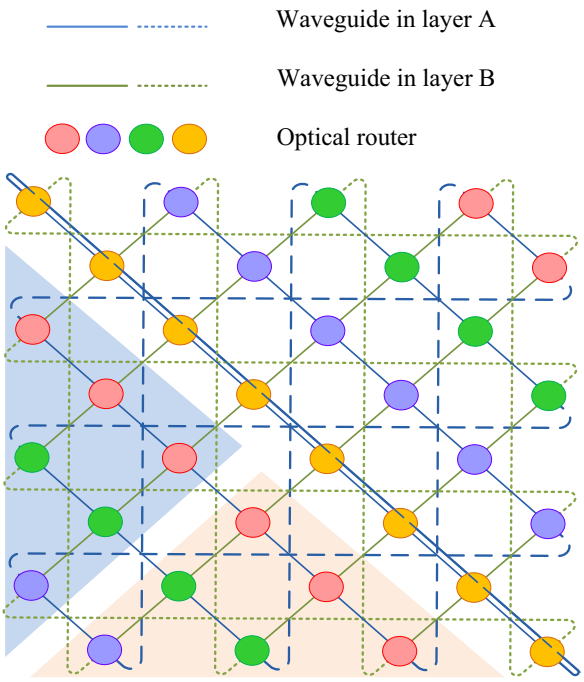

Fig. 2. Subnet 0 topology.