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Energy efficient network design tool for green IP/Ethernet networks

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ABSTRACT

An innovative energy-efficient network design algorithm and a tool to lower the network power consumption are proposed. The goal is an energy efficient network that carries its rated communication load while meeting the QoS requirements by using the minimum set of nodes and links. OoS metrics include hop limit, bandwidth limit reliability and stability. The proposed algorithm addresses the set-covered problem. To discover the optimum network configuration efficiently, we propose a network configuration generation algorithm that utilizes DAPDNA-2, a parallel data flow type reconfigurable processer. The processor automatically produces the node/link set in n-digit binary form where links are modeled as "1" for power on and "0" for power off; it also confirms that the OoS requirements are satisfied. Evaluation results show that DAPDNA-2 is 2-orders faster than the conventional sequential method running on a Pentium-4 processor. Prototype Gigabit Layer-2 switches having remote link power on/off and traffic monitoring functions are developed. Using these switches, we successfully demonstrate an energy efficient IP/Ethernet network. The evaluation results show that network power savings of up to 30% can be realized under the NFSNET topology model. The proposed algorithm and power efficient network architecture can be applied to realize the future green network.

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1. Introduction

The continued growth in the Internet service means that network throughput must be raised significantly. In particular, video data transfer and rich web services are generating heavy traffic loads. This will only further increase the energy consumed by IT equipment. Fig. 1 shows the energy consumption forecasts for IT equipment in Japan. According to this figure, power consumed by routers will increase dramatically [1]. In 2010, 13,000 million kwh/year (13 TWh/year) will be consumed. That is equivalent to two nuclear power plants.

To reduce network energy consumption, several techniques are being developed. The first one, by IEEE, is the Energy Efficient Ethernet (EEE). This technique changes link

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speed according to the data traffic demand. The second is to employ low power voltage LSIs. The third is to use DC power supply to reduce AC/DC conversion loss. The fourth is to use a network virtualization technique such as virtual servers and virtual routers.

We proposed the energy efficient network control concept named "MiDORi (Multi- (layer, path, and resources) Dynamically Optimized Routing). "Midori" is the Japanese word for "green" [2]. To reduce the power consumption, we control the power off/on state of links and nodes. This operation is controlled by a Path Computation Engine/Element (PCE). A low energy consumption network design engine in the PCE determines the optimal network topology (path routes). IP routers/Ethernet switches are controlled by this PCE via GMPLS (Generalized Multi-Protocol Label Switching) based link power on/off control protocols [2].

This paper proposes a new energy efficient network design tool for IP/ Ethernet networks. The proposed tool



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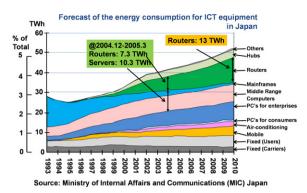


Fig. 1. Energy consumption for IT equipment from. Asami and Namiki, ECOC 2008, Tu.4.A.3, Brussels, Belgium, Sept. 23, 2008 [1].

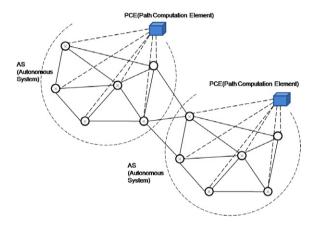


Fig. 2. Basic network configuration using PCE for path control in the AS.

aggregates the traffic and powers down empty links by monitoring the amount of traffic being transferred in the network. In other words, by activating the fewest possible links at any one time, the network topology can be dynamically reconfigured in an energy saving manner.

The rest of the paper is organized as follows. In Section 2, the concept of the low power consumption network architecture is presented. Section 3 details the energy efficient network topology generation algorithm and its evaluation. Required link on/off protocol is proposed in Section 4. Section 5 presents the prototype Gigabit Layer-2 switch. Finally in Section 6, we summarize the paper.

2. Low power consumption network architecture

Today's network structure is shown in Fig. 2. The network consists of ASs (Autonomous Systems) which includes tens to hundreds of routers with controllers. The network topology (path routes) is controlled by PCE. PCE calculates network topology to match traffic demands and network conditions. Our research target is a high-performance PCE that can efficiently calculate the network topology with the lowest power consumption and control the power off/on states of links and nodes.

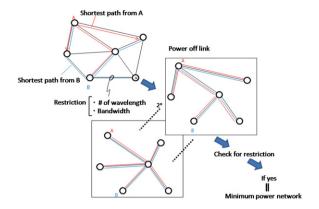


Fig. 3. Optimum network topology for low power consumption.

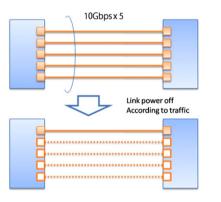


Fig. 4. Power off technique for parallel links.

The key energy saving approaches are as follows [3];

2.1. Interface power off

Some parallel links and single links are deactivated if the traffic demand is low. In that case, both sides of the interface are automatically powered off. In addition, PCE considers these links as sleeping links; they physically exist but are inactive.

2.2. Node power off and partial power off

Transits routers that are not currently needed are powered off, low traffic routers will be partially powered off. Partially powering off a router is realized by partially deactivating the switch fabric and controllers.

Proposed design method is illustrated in Fig. 3 for the case of 6 nodes and n links. First, with regard to on/off states, total link combination number is 2^n . The initial topology has all links powered off, so nodes cannot communicate with each other. Next, one link is powered on, this pattern has n combinations. Additional links can be powered on one by one. The network topology pattern that can carry all traffic demands is selected. With regard to routers, router power consumption is proportional to the traffic amount, and the traffic of a low load router can be moved to another router and the empty router can be powered off. Download English Version:

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