Optical Switching and Networking 18 (2015) 201–210

Contents lists available at ScienceDirect

Optical Switching and Networking

journal homepage: www.elsevier.com/locate/osn

Queueing analysis of optical and electronic combined buffer for optical packet switches

Takahiro Hirayama*, Takaya Miyazawa, Hiroaki Harai

National Institute of Information and Communications Technology (NICT), 4-2-1 Nukui-Kitamachi, Koganei-shi, Tokyo 184-8795, Japan

ARTICLE INFO

Article history:
Received 20 February 2015
Received in revised form
15 July 2015
Accepted 23 August 2015
Available online 3 September 2015

Keywords:
Optical packet switch
FDL buffer
Analytical model
Queueing theory

ABSTRACT

Optical packet switching provides high-speed and energy-efficient packet forwarding. Fiber delay line (FDL)-based buffer is one practical solution to avoid packet contention in optical packet switches. However, the FDL buffer suffers from scalability problems, and thus, cannot accommodate a large volume of network traffic at a time. An optical and electronic combined (OE) buffer architecture alleviates the scalability issues. This architecture uses supplementary electronic RAM buffers when the traffic volume increases. We then propose an analytical model of the OE buffer to estimate the blocking probability and the average delay. We find that complex OE combined model can be simply modeled by combination of an existing analytic model of the FDL buffer and an $M/M/1/K$ queueing system. Comparing analytical results with packet-level simulation results, we demonstrate that our analytical results display characteristics similar to the simulation results. This analysis enables to determine appropriate setting of the OE buffer such as the buffer size and use policy.

1. Introduction

The packet forwarding systems currently used need to be further improved in preparation for an anticipated increase in the Internet traffic in the future. However, improving computation power of electronic packet switching systems is difficult. Furthermore, electronic switches consume tremendous amount of energy with increasing computation power. To solve this issue, optical packet switching has received much attention. Optical packet switches (OPSs) provide high-speed and energy-efficient packet forwarding because there is no need for optical–electronic (O/E) and electronic–optical (E/O) signal conversion.

Fiber-delay-line (FDL)-based buffer architecture is one solution for OPSs. Basically, an FDL buffer consists of multiple FDLs with different fiber lengths and avoids packet collisions by adding delays to successive packets. The FDL buffer has been focused as a more practical approach to the implementation of OPSs than optical RAMs. So far, many researchers proposed methods for high-speed buffer management systems [1–7]. Previously, the largest size of the FDL buffers in experiments is a 31-FDL buffer consisting cascaded PLZT switches [8]. In addition, we have demonstrated transport of 100-Gbps IP-packet-encapsulated optical packets with an SOA-based 8-FDL buffer [9].

However, it is difficult to enhance the capacity of an FDL buffer. As the number of FDLs increases, the buffer requires a large chassis and a large number of highly accurate optical devices such as optical splitters, couplers, and amplifiers. There are technical and economic constraints for these requirements. In order to deal with the scalability problem,

* Corresponding authors.
E-mail addresses: hirayama@nict.go.jp (T. Hirayama), takaya@nict.go.jp (T. Miyazawa), harai@nict.go.jp (H. Harai).

http://dx.doi.org/10.1016/j.osn.2015.08.003
1573-4277/

different types of FDL buffers have been proposed in the literature. One of them is shared buffer architecture, where each output port shares one large FDL buffer [2–6,10]. However, it is hard to manage the large shared buffer. In contrast, managing dedicated buffer is easier than managing the shared buffer. Hence, we proposed dedicated buffer architecture where each output port has a small FDL buffer and a supplementary electronic RAM buffer [11,12]. This optical and electronic combined (OE) buffer architecture, in which optical buffer and electronic buffer are combined, keeps the FDL buffer size small by taking advantage of the electronic buffer when traffic increases. We have demonstrated that the proposed buffer architecture obtains 70% larger throughput than that of the existing FDL buffer. Furthermore, compared with the shared buffer, the OE buffer can reduce its management complexity, and also reduces the costs of optical devices due to the fewer number of FDLs required. However, there are many things that need to be considered in designing and managing the OE buffer, e.g., the number of FDLs, and the threshold that indicates whether electronic RAMs are required or not. Many combinations of system parameters have to be evaluated to determine an appropriate setting of the OE buffer.

Analytic models are helpful in designing network components such as the buffer size and computation resources. There are many studies reported on analytic models of basic FDL buffer architecture consisting of B FDLs (where B represents the number of FDLs) [13–18]. The length of each FDL is an integer multiple the unit length D [ns] (0, D, $2D$, …, $(B-1)D$), thus the FDL buffer provides discrete-time delays from 0 to $(B-1)D$ [ns]. Due to the *discrete*-time nature of FDL buffer, a void space exists between adjacent outgoing packets in a fiber. Furthermore, whether a packet is accepted or rejected depends on the maximum length of the FDLs. The analytic models discussed in [13–18] incorporate the features of FDL buffers. Analytic models of other types of FDL buffers such as shared buffer and feedback buffer have been also discussed in [19–21]. However, analytic models of the OE buffer have not been reported in any literature, even though the OE buffer possesses performance advantages.

In this paper, we propose an analytic model of the OE buffer architecture. The model is based on the results of existing analytic models of FDL buffer (e.g., [15,16]) and an $M/M/1/K$ queueing model applied to an electronic buffer. Our analytic model provides estimates of the packet loss probability and average queueing delay of the OE buffer. Network designers can easily determine the buffer capacity required for a prescribed packet loss probability. We compare analytical results and simulation results for a given set of constraints for implementation. This comparison indicates that the analytic models tend to overdesign the required buffer size, in the region where the prescribed packet loss probability is very small. However, the model is useful for designing the OE buffers because it can determine the range of offered load where the combined buffer works well.

This paper is organized as follows. In Section 2, we explain the architecture of the basic FDL buffer and the OE buffer. And then, we describe their behavior. Our analytic model is described in details in Section 3 and is compared with simulation results in Section 4. We conclude this paper in Section 5.

2. Optical and electronic combined buffer architecture

2.1. FDL buffer architecture

In this section, we discuss both dedicated FDL buffer architecture and shared one, which are illustrated in Fig. 1. An $N \times N$ OPS with a dedicated buffer (Fig. 1(a)) consist of N switches of size $1 \times N$ and N buffers of size $N \times 1$. All the $1 \times N$ switches and $N \times 1$ buffers are interconnected in a fully meshed manner. Every output port has its dedicated FDL buffer as shown in the lower part of Fig. 1(a). The FDL buffer is composed of an $N \times (B/N)$ optical switch and B/N FDLs. The length of the B/N FDLs is a multiple of the unit length D [ns] (0, D, $2D$, …, $(B/N-1)D$).

In contrast with the dedicated buffer discussed above, a shared FDL buffer consists of a large optical switch and FDL buffers. Two types of shared FDL buffers are considered here. Feedback shared buffer architecture is composed of an $(N+B) \times (N+B)$ optical switch and B FDL buffers (shown in Fig. 1(b)). Similar to the dedicated buffer, different FDLs have different lengths. A packet arriving at a certain input port is recycled to the shared buffer when a possibility of packet collision is detected at the destination port. When a packet goes out of the buffer, the packet is guided to its destination port if the port is idle. If the destination port is occupied, the packet is rerouted to the buffer again. Note that a packet is

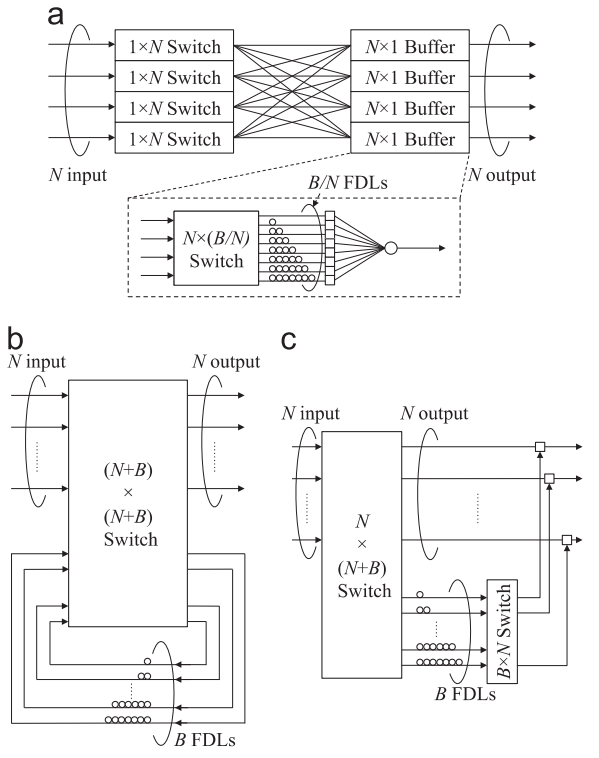

Fig. 1. Examples of FDL buffer architecture.