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A novel approach to hedge and compensate the critical dimension variation of the developed-and-etched circuit patterns for yield enhancement in semiconductor manufacturing

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ABSTRACT

Linewidth control is critical for yield enhancement in semiconductor manufacturing. As wafer fabrication reaching nano-technology nodes, existing approaches on advanced equipment control and advanced process control (AEC/APC) for variation control of individual processes are increasingly difficult to achieve desired process control due to shrinking process windows. This study aims to propose a novel approach to determine tool affinity to hedge the variation between the photolithography for pattern development and the etching process to effectively reduce the etching bias caused by tool misalignment. In particular, the proposed approach integrates a feed-forward run-to-run (R2R) controller and the proposed mini-max regret tool dispatching rules in light of the tool characteristics of the photolithography and etching processes. To validate the proposed approach, an empirical study was conducted in a leading semiconductor company in Taiwan and the results showed practical viability of the approach.

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1. Introduction

With the shrinking feature size of integrated circuits (ICs) driven by Moore's Law [1], the tighter critical dimension (CD) control is increasingly critical for yield enhancement as wafer fabrication reaching advanced technology nodes of 28 nm/20 nm. The CD is the minimum width of patterned lines or the distance between two pattern lines [2]. Wafer fabrication contains hundreds of process steps, in which photolithography and etching are two critical processes for determining CD that affects the yield. In particular, the CD of developed patterns *via* photolithography processes is called the developed critical dimension (DCD). The CD measured by the metrology after the etching process is called the etched critical dimension (ECD). The ECD represents the final linewidth of fabricated patterns of each layer on the wafer, in which the variation of both DCD and ECD will directly affect process yield and product quality. The CD variation contains within-wafer variability including field-to-field and site-to-site, wafer-to-wafer variability, lot-to-lot variability and the variability caused by different tool behaviors [7,13]. The within-wafer variability that is a consequence of reactor design usually represented as an issue of non-uniformity. Wafer-to-wafer variability and lot-to-lot variability are caused by poor repeatability of the equipment or process on the incoming wafers. In addition, the misalignment between the upstream photolithography and the downstream etching tools may amplify the variation of fabricated patterns on the wafer. As the tolerance for process spec is reduced in nano-technology nodes and the number of parallel production tools (and chambers) for wafer fabrication is increasing, the present problem is becoming critical for yield enhancement.

To reduce CD variation for yield enhancement, advanced equipment control and advanced process control (AEC/APC) with run-to-run (R2R) controllers have been widely adopted in different wafer fabrication processes such as photolithography and etching [3–12]. For example, Ho et al. [8] reduced the DCD non-uniformity through real-time photoresist thickness control by controlling softbake temperature in photolithography. Zhang et al. [9] enhanced the uniformity of both DCD and ECD by manipulating the temperature of post exposure bake (PEB) in photolithography. In addition, the exposure dose and focus were two influential factors for DCD control [3], in which various feedback controllers based on exponentially weighted moving average (EWMA) estimation or Kalman filters were proposed [6]. For ECD control, existing studies considered two modeling responses, *i.e.*, ECD measurement [6,10,11] and the etching bias [5,7,12], and the variables for manipulation including etching time [6,10,12], oxygen flow rate [11], and the peak radio-frequency (RF) voltage

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[7]. However, most of the existing approaches focused on employing AEC/APC for variation control of individual processes that are increasingly difficult in nano-technology nodes. Little research has been done to address the present problem for reducing ECD variation *via* considering the covariance of DCD and ECD caused by different tools and chambers to reduce the bias *via* tool matching and production control in a short process loop of etching processes.

Focusing on the needs to reduce the variation of etched patterns in real settings, this study aims to propose a novel approach to hedge the variation of pattern development and etching processes to compensate the variation for ECD control while considering production effectiveness. The proposed framework integrates a feed-forward R2R controller and dispatching rules for matching the tools for pattern development and etching based on the corresponding tool characteristics. In particular, the developed approach has modeled and estimated the chamber effects on the etching bias to construct a dissimilarity measurement for real-time tool dispatching for matching the tools to reduce ECD variation between the tools (chambers). Although scheduling and dispatching have been important issues for semiconductor manufacturing with multiple objectives [13–15], few studies have considered both productivity and process control. An empirical study was conducted to validate the proposed approach in a leading semiconductor company in Taiwan. The results have shown the practical viability of the proposed approach.

The remainder of this study is organized as follows. Section 2 introduces the fundamentals of critical dimensions, AEC/APC, and the control hierarchy in semiconductor manufacturing. Section 3 describes the proposed approach. Section 4 validates the proposed approach with an empirical study. Section 5 concludes this study with a discussion and suggestions for further research.

2. Fundamentals

2.1. Short loop for determining critical dimension

Photolithography and etching are two process modules related to CD determination and control in the semiconductor fabrication. In particular, the photolithography process is employed to develop the mask pattern on the PR layer through a sequence of process steps including dehydration back, priming, spin coating, soft bake, exposure, post exposure bake, development, and hard bake. Among these steps, various factors including spin speed, baking temperature, baking time, dose, focus, and develop time may affect the results of DCD measurement that is defined as the width of the positive photoresist as shown in Fig. 1(a). The etching process is employed to etch the thin film that is not coated by positive photoresist to form the mask pattern on the wafer surface for each layer as shown in Fig. 1(b). The etching time of endpoint detection will affect ECD measurement. Then, the residual photoresist will be removed from the etched wafer to measure the ECD.

In practice, both DCD and ECD are measured by metrology tools based on a sampling plan to estimate the mean CD for a lot. The sampling plan determines the number of sampling wafers in a lot, number of sampling fields and their locations on a wafer, and number of sampling sites, and their positions on an exposure field [16]. For example, research has been done to design the optimal sampling strategy with a limited number of selected sites for measuring and compensating overlay errors for process control and yield enhancement [17,18]. To enhance the performance and accuracy of APC, Asano and Ikeda [19] studied the sources of CD errors and proposed an optimal sampling plan based on CD mean estimation using analysis of variance (ANOVA). Vincent et al. [20] used modeling and minimum-variance prediction based on principal component analysis and canonical correlation analysis to select the sampled sites on the wafer for metrology for process control.

However, it is increasingly difficult to control CD variation within the shrinking process window for quality control of individual processes in nano-technology nodes. This study defines the etching bias as the difference between ECD and DCD measurement that can be used to reduce the variation of etched patterns *via* matching tools in etching processes. The chamber effects on the etching bias will be modeled to construct a dissimilarity measurement for real-time tool dispatching for matching the tools for photolithography and etching to reduce ECD variation.

2.2. Advanced equipment control/advanced process control

Advanced equipment control/advanced process control (AEC/APC) is a collection of methodologies including run-to-run (R2R) control, fault detection and classification (FDC), and virtual metrology (VM) to reduce process variation and meet process target for yield enhancement. This desired process results are achieved by automatically manipulating process recipes and/or equipment parameters based on *ex-situ* metrology data and/or real-time (*in-situ*) monitoring tool-level data [21]. In particular, Moyne et al. [22,23] defined R2R control as a form of discrete process and machine control, in which the product recipe with respect to a particular machine process is modified *ex-situ*, *i.e.*, between machine “runs”, to minimize process drift, shift, and variability. A “run” can be a single wafer, a lot, a batch, or any other grouping of semiconductor products undergoing the same set of process conditions. To achieve desired process output results, R2R control systems involve both feed-forward and feedback control schemes. R2R controllers are generally implemented through EWMA-based algorithms [24].

Semiconductor process control consists of several levels including real-time control, single-process R2R control, inter-process

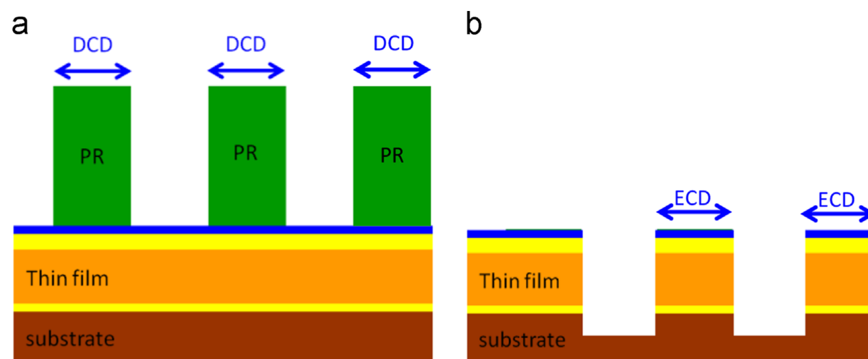

Fig. 1. The DCD/ECD measurement.

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