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Multiple-valued logic design based on the multiple-peak BiCMOS-NDR circuits

Kwang-Jow Gan [a,*], Jeng-Jong Lu [b], Wen-Kuan Yeh [c], Yaw-Hwang Chen [d], Yan-Wun Chen [d]

[a] Department of Electrical Engineering, National Chiayi University, No. 300, Syuefu Rd., Chiayi City 60004, Taiwan
[b] Department of Mechanical Engineering, Kun Shan University, No.195, Kunda Rd., YongKang Dist., Tainan City 71003, Taiwan
[c] Department of Electrical Engineering, National University of Kaohsiung, No. 700, Kaohsiung University Rd., Nanzih Dist., Kaohsiung 81148, Taiwan
[d] Department of Electronic Engineering, Kun Shan University, No.195, Kunda Rd., YongKang Dist., Tainan City 71003, Taiwan

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ABSTRACT

Three different multiple-valued logic (MVL) designs using the multiple-peak negative-differential-resistance (NDR) circuits are investigated. The basic NDR element, which is made of several Si-based metal-oxide-semiconductor field-effect-transistor (MOS) and SiGe-based heterojunction-bipolar-transistor (HBT) devices, can be implemented by using a standard BiCMOS process. These MVL circuits are designed based on the triggering-pulse control, saw-tooth input signal, and peak-control methods, respectively. However, there are some transient states existing between the multiple stable levels for the first two methods. These states might affect the circuit function in practical application. As a result, our proposed peak-control method for the MVL design can be used to overcome these transient states.

1. Introduction

Multiple-valued logic (MVL) circuits offer several potential applications for the improvement of modern circuit designs. The origin of MVL was from the Lukasiewicz logic idea [1]. The MVL can transfer more information with fewer interconnects between devices as compared to traditional binary logic. We can use the MVL domain for more efficient solution of binary problem, thus achieving high-speed arithmetic operations. It can also provide more compact solutions and better functional capabilities in the information process [2,3].

MVL circuits could be implemented in bipolar technology such as integrated injection logic (I^2L) [4] and emitter-coupled logic (ECL) [5]. Because the silicon gate MOS transistor replaced bipolar circuits as the main device in circuit design, there were some reports that used the MOS or CMOS technology to design the MVL circuits [6–10]. There were two main technologies such as current mode [11] and voltage mode [12], which could be used to design the MOS-based MVL circuits. Recently, the carbon nanotube was used to design the MVL circuits [13,14]. Among these technologies, there are two potential candidates for commercial purposes, which are current-mode CMOS technology and negative-differential-resistance devices [15].

The negative differential resistance (NDR) device has remarkable property due to its folded current–voltage (I–V) curve. The well-known NDR devices are Esaki diode and resonant-tunneling diode (RTD). Their NDR characteristics can provide very attractive and useful ideas for some applications [16–18]. In particular, the multiple-peak NDR circuits provide the convenience to design the MVL circuits. Several MVL circuits were demonstrated by using the RTD [19,20], the resonant interband tunneling diode (RITD) [21], and quantum dot gate FETs [22].

The RTD made by III–V materials including GaAs and InP is not compatible with the mainstream ULSI technology, such as the CMOS or BiCMOS process. The fabrication of the RTD-based applications involves the use of the molecular-beam-epitaxy (MBE) or metal-organic-chemical-vapor-deposition (MOCVD) system. If the RTD-based applications need to integrate with the Si-based active and passive devices to achieve the system on a chip, the process for the integration of the MOCVD system with the CMOS technique is not easy. This limits the development of the RTD-based applications. Therefore, if we can fabricate the NDR-based circuits using the CMOS or BiCMOS technique, it is very attractive in the commercial applications. Besides, the circuit can be simulated using the HSPICE program, which is the most popular CAD tool in the IC design.

In recent years, there were some reports on Si-based RITD structures [23,24], and some of them were successfully integrated with the Si-based CMOS [25] and the SiGe heterojunction-bipolar-transistor (HBT) [26], making these devices promising for future applications. However, they still need the MBE system to

* Corresponding author. Tel.: +886 5 2717588, fax: +886 5 2717558.
E-mail address: gankj@ms52.hinet.net (K.-J. Gan).
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accomplish the combined circuits and applications. In this work, we propose a MOS-HBT-NDR NDR circuit, which is made of several standard Si-based MOS devices and SiGe-based HBT devices. A four-valued logic circuit is demonstrated using a three-peak NDR curve that is made of three series-connected MOS-HBT-NDR circuits.

A traditional NDR-based MVL circuit requires a load device to bias the multiple-peak NDR circuit to obtain the stable logic states. We present three different MVL designs by using a resistor as a load, because it is a simple and direct method. However, the first two circuits showed that some transient states existed in the output results. Those transient states were located between the stable states. The states were so high that they might result in error transfer in the information system. To overcome this problem, we designed the third MVL circuit using the voltage-controlled MOS-HBT-NDR circuit, where the peaks of the multiple-peak I–V characteristics could be controlled by the external voltages. Using this method, we designed a voltage-controlled MVL circuit with four clear logic states, and there was no transient state occurring between two stable states. This NDR-based MVL circuit was designed according to the standard SiGe BiCMOS process provided by the Taiwan Semiconductor Manufacturing Company (TSMC) foundry.

2. Basic NDR and MVL circuit design

The MOS-HBT-NDR circuit used in this work is made of three Si-based n-channel MOS and one SiGe-based HBT devices, as shown in Fig. 1. The circuit can show the NDR I–V characteristic by determining the appropriate gate width/length (W/L) parameters of the MOS devices. In view of the operation of this MOS-HBT-NDR circuit, we should apply a fixed voltage Vgg and increase the bias V_S gradually. The magnitude of the Vgg must be larger than the sum of threshold voltage of the MN1 device and the turn-on voltage of the HBT device. The MN1 device is connected like a diode and is always turned on during circuit operation. The MN2 device is operated as a variable resistor as we increase the bias V_S gradually. The combined current is the sum of the collector current of the HBT device and the drain current of the MN3 device. Because the MN1 and MN2 devices can be regarded as a voltage divider, the node voltage between them can be used to control the operation situation of the HBT device.

When we apply a small voltage V_S, the operation of the MN1 device is saturated and the MN2 device is turned off. The current is proportional to this voltage. This region is the first positive-differential-resistance (PDR) segment of the combined I–V curve. If we further increase the bias V_S, the MN2 device is turned on and the base voltage of the HBT device is decreased gradually. It results in the decrease of the collector current gradually. This region is the NDR segment of the combined I–V curve. Finally, the bias V_S is high enough to make both the MN1 and MN2 devices saturated. When the node voltage between the MN1 and the MN2 devices is smaller

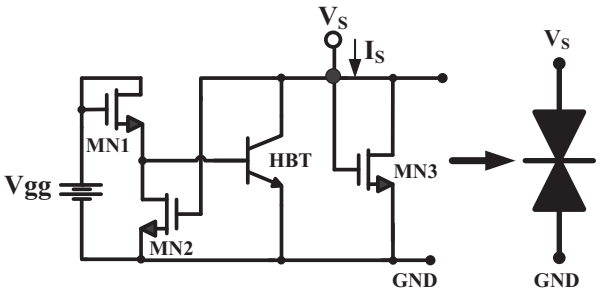

Fig. 1. Circuit configuration of a MOS-HBT-NDR circuit.

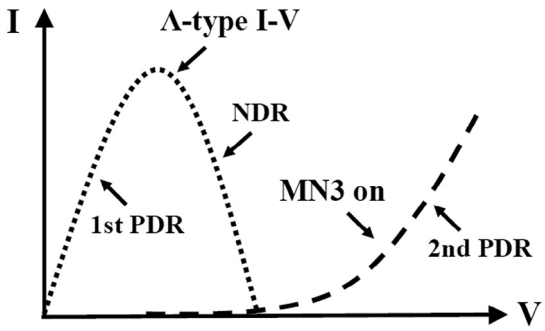

Fig. 2. I–V characteristic of a MOS-HBT-NDR circuit.

than the turn-on voltage of the HBT device, the HBT device is turned off. Therefore, the combined current of the MN1, MN2, and HBT devices is presented as a Λ-type I–V characteristic, as the dotted lines shown in Fig. 2.

The MN3 device is connected like a diode and controlled by the bias V_S. When the bias V_S is larger than the threshold voltage, its I–V characteristic is an exponential curve, as the broken lines shown in Fig. 2. This establishes the second PDR segment of the combined I–V characteristic. Finally, we can obtain an N-type I–V curve in the combined NDR circuit by increasing the bias V_S gradually. Notice that the NMOS of the MN1 and MN3 devices can be replaced by the PMOS devices. The HBT device can be replaced by the BJT or NMOS device. Therefore, this NDR circuit can be implemented by using the CMOS or BiCMOS technique.

In particular, this NDR circuit possesses the ability to control the peak current by the external voltage terminal Vgg. If we increase the voltage Vgg, the base voltage of the HBT device is increased too. This results in the increase of the collector current of the HBT device. Therefore, we can obtain higher peak current. Fig. 3 shows the simulated I–V characteristics by varying the Vgg values from 1.5 V to 2.7 V with a step of 0.2 V. The MOS parameters were designed as $W_{MN1} = 3\ \mu m$, $W_{MN2} = 10\ \mu m$, $W_{MN3} = 10\ \mu m$ and $L_{MN1,2,3} = 0.35\ \mu m$. The HBT was used the standard ln02 cell based on the standard 0.35 μm SiGe process provided by the TSMC foundry. When the Vgg is biased at 2.1 V, the simulated peak voltage is 0.55 V, valley voltage is 0.85 V, peak current is 2 mA, and valley current is 0.25 mA. The peak-to-valley current ratio (PVCR) is about 8.

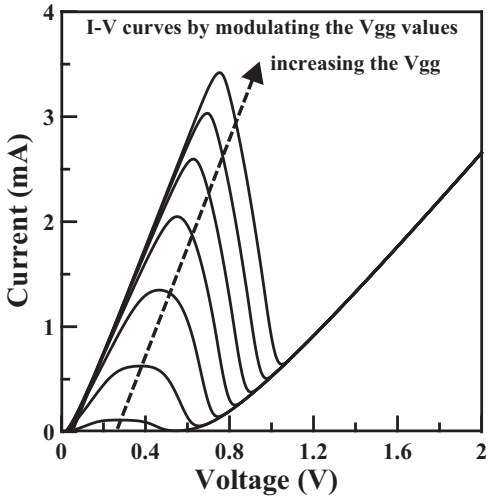

Fig. 3. I–V characteristics of a MOS-HBT-NDR circuit by modulating the Vgg values.