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Full Length Article

Design, implementation and performance comparison of multiplier topologies in power-delay space

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ABSTRACT

With the advancements in the semiconductor industry, designing a high performance processor is a prime concern. Multiplier is one of the most crucial parts in almost every digital signal processing applications. This paper addresses the implementation of an 8-bit multiplier design employing CMOS full adder, full adder using Double Pass Transistor (DPL) and multioutput carry Lookahead logic (CLA). DPL adder avoids the noise margin problem and speed degradation at low value of supply voltages associated with complementary pass transistor (CPL) logic circuits. Multioutput carry lookahead adder leads to significant improvement in the speed of the overall circuitry. The investigation is carried out with simulation runs on HSPICE environment using 90 nm process technology at 25 °C. Finally, the design guidelines are derived to select the most suitable topology for the desired applications. Investigation reveals that multiplier design using multioutput carry lookahead adder proves to be more speed efficient in comparison with the other two considered design strategies.

1. Introduction

The integrated circuit designers are facing new challenges due to the exponential growth in electronic devices and equipments in the past few years. Addition of more functionality along with real time applications demands revolutionary changes in the design process of a chip. Increase in computing requirements onto a single chip demands development of sophisticated tools that can perform complex operations which further results in increase in the processing power. Thus, development of high speed computational hardware i.e., adders and multipliers, is a prime concern in today's scenario. For low power and real time applications, computationally intensive digital signal processing algorithms are implemented in dedicated VLSI systems. Multiplier is one of the most crucial parts in such systems. The computation speed of processor is highly dependent on these arithmetic units. High performance processors result in increase in the complexity of the design. In order to improve the performance of processors there is a need to improve the complexity of such arithmetic units. Recent developments in portable electronic devices and digital signal processing systems demand flexible computational ability, low power utilization and shorter design cycles. Two most important design criteria deciding the performance of processor are speed and power consumption. In the literature many research efforts have been carried out in order to obtain energy efficient multiplier and adder architectures as demonstrated [1–7]. State-of-the-art designs focused mainly on reducing the silicon area but in the last decade the focus is primarily shifted toward speed and power. The complexity of the design directly depends on the speed of computation. High speed requirement results in increased complexity of the circuit, hence larger number of transistors will be required in the design which further results in high power dissipation. So there is a tradeoff between speed and power dissipation.

Adder is the basic component in any computational hardware. Thus, its performance characteristics directly affect the functioning of the entire system. Therefore, improvement in the performance of adder architecture is a prime concern as reported [8]. Various techniques can be employed externally or internally in order to improve the overall performance of any system. External techniques involve dealing with input data characteristics whereas internal techniques are concerned with the logic, circuit design and architecture of multiplier as reported [9–13]. The basic element of a multiplier design is the adder cell, which significantly affects the overall performance characteristics of a multiplier. The recent advancements in CMOS technology indicate a strong need for high speed, high density, low power, low cost multiplier design for

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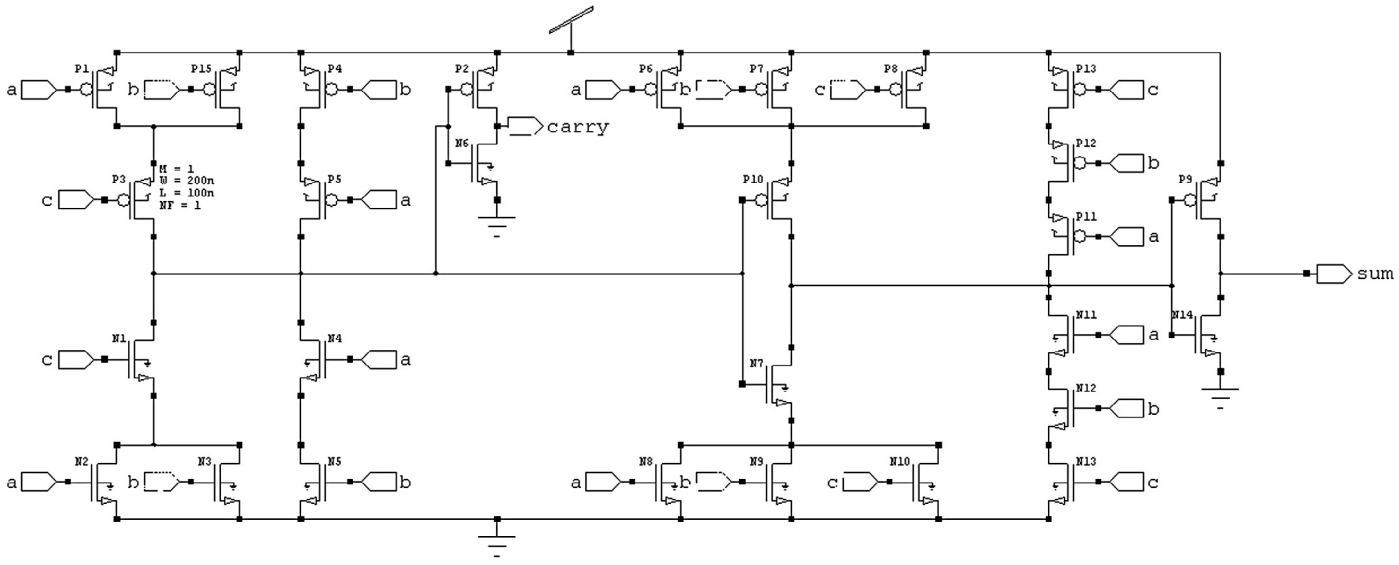

Fig. 1. Schematic of full adder.

ubiquitous use in majority of leading-edge commercial applications. In this paper an 8-bit Multiplier is designed with three different adder architectures i.e. CMOS full adder, Double Pass Transistor logic (DPL) as proposed by References 14 and 15 and multioutput Carry Lookahead (CLA) adder as demonstrated by Reference 16 and detailed analysis is carried out in terms of delay, power and power delay product (PDP). This paper proposes an 8-bit multiplier design using High speed multioutput CLA adders.

The remainder of this paper is organized as follows. In section 2, 8-bit adders are addressed using three different logic styles: CMOS full adder, DPL full adder and domino multioutput CLA adder architecture. In section 3, multiplier architectures are presented. Section 4 presents the comparison of the 8-bit full adders and 8-bit multipliers. Finally, in section 5, the conclusions are drawn.

2. Adder topologies analyzed

Adder is the basic architecture commonly used in every arithmetic circuit. In a multiplier design adders are used for partial product addition, and thus contribute toward the largest part of delay associated with whole multiplication process. This section presents different types of adders considered in this research.

2.1. CMOS full adder

CMOS full adder design is implemented using stack of PMOS and NMOS transistors. The basic architecture of full adder design consists of 28 transistors and three input variables (*a*, *b* and *c*) and two output variables (*sum* and *carry*) of 1-bit each. The schematic of full adder is shown in Fig. 1. The two outputs of the adder *sum* and *carry* are represented as:

$$\text{Sum} = a \oplus b \oplus c$$
$$\text{Carry} = a.b + b.c + c.a$$

The 8-bit ripple carry adder consists of eight full adder cells in cascade such that output carry of one full adder cell is applied as an input carry to another full adder cell. The architecture of an 8-bit ripple carry adder is shown in Fig. 2. Eight inputs a_7 to a_0 and b_7 to b_0 are applied to each of the full adder cell and output S_7 to S_0 represents eight bit sum from each full adder. The input carry of the first half adder cell must be grounded for the correct addition of least significant bits (a_0, b_0) otherwise it will result in erroneous output. As the whole computation solely relies on carry rippling, it results in large value of delay overhead. However ripple carry adder is one of the simplest adder architecture and requires less power consumption and area.

2.2. Double pass transistor logic (DPL) adder

Double pass transistor is a type of Pass transistor logic style. It is a modified version of complementary Pass transistor logic (CPL). CPL consists of only NMOS pass transistors, whereas the modified version DPL has both NMOS and PMOS transistors in symmetry in order to achieve full swing output from 0 to V_{DD} and reduced supply voltage.

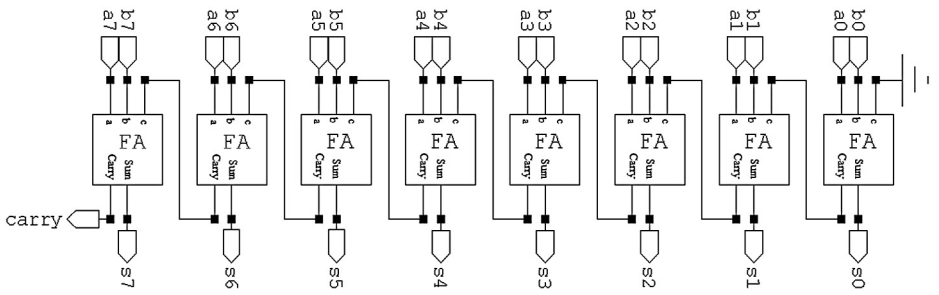

Fig. 2. Eight-bit Ripple Carry adder.