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Analytical study of Dual Material Surrounding Gate MOSFET to suppress short-channel effects (SCEs)

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ABSTRACT

In this paper, a 2D analytical model for the Dual Material Surrounding Gate MOSFET (DMSG) by solving the Poisson equation has been proposed and verified using ATLAS TCAD device simulator. Analytical modeling of parameters like threshold voltage, surface potential and Electric field distribution is developed using parabolic approximation method. A comparative study of the SCEs for DMSG and SMSG device structures of same dimensions has been carried out. Result reveals that DMSG MOSFET provides higher efficacy to prevent short-channel effects (SCEs) as compared to a conventional SMSG MOSFET due to the presence of the perceivable step in the surface potential profile which effectively screen the drain potential variation in the source side of the channel. A nice agreement between the results obtained from the model and the results obtained from numerical TCAD device simulator provides the validity and correctness of the developed model.

1. Introduction

Increased short-channel effects (SCEs) appear as a major roadblock to maintain the performance enhancement in conventional bulk Si MOSFETs with deca-nanometer technology node. According to ITRS [1], incorporation of new technologies is becoming crucial for deep sub-micron CMOS devices. Among different possible solutions, non-conventional MOSFET device structure employing the gate-material engineering [2] improves the gate transport efficiency by modifying the electric field pattern and the surface potential along the channel, resulting in higher carrier transport efficiency, higher transconductance and SCEs suppression. In 1999, a new type of FET structure, proposed by Long et al. [3] is that the dual-material gate (DMG) FET, employing "gate-material engineering" to improve both carrier transport efficiency and SCEs. The gate material with higher workfunction near the source end acts as the "control gate", while the gate material with lower workfunction near the drain end acts as the "screening gate" that prevents any changes in the drain bias to affect the channel region under the first gate. In the DMG MOSFET, two metals M_1 and M_2 of different workfunction are amalgamated together laterally. The workfunction of M_1 is greater than M_2 i.e. $\Phi_{M1} > \Phi_{M2}$. Such a configuration introduces a step function in the potential along the channel such that the electric field distribution is enhanced at the source side to increase the carrier velocity while the drain potential change will be screened. Work function in M_2 is chosen greater than M_1 for a p-channel MOSFET and vice-versa for an n-channel MOSFET. In spite of the several benefits offered by gate-material engineering, the major issue of concern is the viability of fabrication. Recently, Sarkar et al. [4] has emphasized the challenges and current status of the fabrication of DMG MOSFET.

Recently, the multiple gate MOSFETs like Double-gate (DG) [5], triple gate [6],FINFET [7] and surrounding gate (SG) [8] MOSFETs has manifested themselves as the most popular candidate for nanoscale design for providing a better scalability option [9]. Excellent short channel effects (SCEs) immunity, high transconductance and near ideal subthreshold slope have been reported by many theoretical and experimental studies on this device [10].

A dual-material double-gate (DM-DG) SOI MOSFETs proposed by Reddy et al. [11] employs gate-material engineering to reduce SCEs significantly when compared to with the DG SOI MOSFET. To get further improvement against SCEs Tiwary et al. [12] proposed TM-DG MOSFET and also developed an analytical subthreshold model. It is inevitable that all variants of FinFETs will finally change to surrounding gate nanowire FETs, because of their best electrostatic gate-control, higher control of SCEs and larger channel area for the nanowire surface per unit area [13–15].

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Yu et al. [16] reported an accurate 2-d analytical model of surrounding gate MOSFET using Bessel functions. On the other hand, surface- potential based model with moderate accuracy such as [17–19] uses the simple polynomial approximation of the potential profile to offer reduced computational burdens and is suitable for the circuit simulation and the device design as compared to Fourier series based approaches [20]. On the other hand, superposition technique based modeling approach was also reported [21], requiring a large computational burden. A computationally efficient modeling based on pseudo-2d approach using Gaussian box in circular coordinates was also proposed [22,23]. Recently Sharma et al. [24] reported a more accurate isomorphic polynomial potential distribution based modeling approach. However, in this study we have chosen parabolic potential based approach due to its simplicity and reduced computational complexity.

To incorporate the advantage of the gate engineering techniques combied with the structural advantage of surrounding gate MOSFET, a novel device structure called Dual Material Surrounding Gate (DMSG) MOSFET is proposed [25]. Later, Chiang et al. reported an analytical subthreshold model using superposition technique [26]. On the other hand, Wang et al. developed a model for triple material surrounding gate MOSFET using superposotion method [27]. Another superposition based model was reported for cylindrical surrounding gate MOSFET [28]. Recently, parabolic potential approach based model of triple material surrounding gate MOSFET was also reported [19]. In this paper, an analytical subthreshold model has been developed to study the effect of gate engineering on surrounding gate MOSFET to reduce SCEs by modeling surface potential, Electric Field, threshold voltage and drain current. Moreover, the effect of radius downscaling on the device performance was observed has also been studied. The analytical modeling demonstrate that DMSG MOSFET structure exhibits significantly enhanced performance in terms of threshold voltage roll-off and DIBL makes it a potential candidate for future generation n-MOSFET based circuits. The results are validated with numerical 2-D device simulation.

2. Model derivation

2.1. Device structure

Fig. 1 shows the 3-d structure of the DMSG n-channel MOSFET considered in this study. In this structure two different gate materials (M_1 and M_2) having different workfunctions (Φ_{M1} and Φ_{M2}) with lengths L_1 and L_2 are amalgamated together to form the gate terminal with total gate length defined as $L = L_1 + L_2$. The gate materials are chosen in such a way ($\Phi_{M1} > \Phi_{M2}$) so that the material with higher workfucntion is kept near the source end functioning as the "control gate" and the material with lower workfucntion is kept near the drain end to function as a "screen gate". Gold (Au $\Phi_{M1} = 4.8$ eV) and Cadmium (Cd) are used as two gate metals to from the gate terminal with their workfunctions 4.8 eV and 4.0 eV respectively. The p-type channel doping level is kept at 6×10^{16} cm^{-3} and for n^+ source/drain regions doping region is chosen as 5×10^{19} cm^{-3} with an abrupt doping profile at the drain/source to channel edges. Hafnium dioxide (HfO_2) is chosen as gate oxide material, in place of conventional SiO_2 ($3.9\varepsilon_0$) due to its higher permittivity ($22\varepsilon_0$) with an Effective Oxide Thickness (EOT) equals to 1.2 nm in order to reduce gate leakage tunneling current [29], where ε_0 denotes the permittivity of the free space. Moreover, it has been demonstrated that as thickness of the oxide reduces, the gate-to-channel capacitance value increases as compared to gate-to-drain capacitance, indicating a higher gate-controllability, resulting in diminished SCEs and better performance [30]. However, beyond 1 nm gate oxide dielectric thickness, the gate-leakage tunneling current becomes significant. Therefore, High-k metal dielectric materials such as HfO_2 with gate-metal stack structures can be considered as a remedy for simultaneous reduction of the gate-leakage current with oxide thickness downscaling [31,32]. The diameter of the Si pillar is chosen $2R = 20$ nm. As we are dealing with devices having radius greater than 5 nm and channel length greater than 10 nm, therefore quantum mechanical effects (QMEs) are negligible [33] and are not considered in this work. Moreover, a ballistic transport model is not considered in this study, as ballistic transport is significant for channel length less than 10 nm [34]. The device parameters are taken according to the International Technology Roadmap for semiconductors 2009 version for low operating power applications [1].

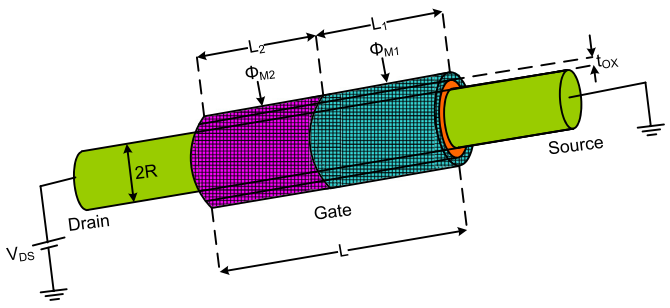

Fig. 1. 3-d structure of a dual material cylindrical surrounding gate MOSFET.

2.2. Model development for surface potential and electric field

Neglecting the influence of mobile charge carriers and fixed trapped charges within the oxide, the 2-d Poisson's equation before the onset of strong inversion can be written as [35]

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial(\phi(r,z))}{\partial r}\right)+\frac{\partial^2(\phi(r,z))}{\partial z^2}=\frac{qN_A}{\varepsilon_{Si}} \quad (1)$$

Where N_A is the acceptor doping concentration of the thin silicon film in (cm^{-3}), ε_{Si} is the relative permittivity of silicon, q is the unit electron charge (1.6×10^{-19}coulomb), $\phi(r,z)$ is the 2D potential distribution in the channel, r is radius of the cylindrical Si film and $z$and is the distance along the channel with reference to the source.

As proposed by Young [36] the potential profile in the axial direction, i.e., the z-dependence of $\phi(r,z)$ can be approximated as simple parabolic function and can be written as

$$\phi(r,z) = c_1(z) + c_2(z)r + c_3(z)r^2 \quad (2)$$

Where the arbitrary coefficients $c_1(z)$, $c_2(z)$ and $c_3(z)$ are to be determined from the following boundary conditions;

1. Surface potential at $r = R$ is a function of z only.

$$\phi(R,z) = \phi_S(z) \quad (3)$$

Where, $\phi_S(z)$ is the surface potential at the Si/SiO_2 interface.

2. Due to radial symmetry the electric field in the center of the cylindrical channel is considered as zero