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The efficiency of buffer and buffer-less data-flow control schemes for congestion avoidance in Networks on Chip

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Abstract The design of efficient architectures for communication in on chip multiprocessors system involves many challenges regarding the internal router functions used in Network on Chip (NoC) infrastructure. The on-chip router should be designed to provide per-flit processing with enhanced granularity. In fact, the quality of service experienced at the application level depends on the capabilities of the router to avoid congestion and to ensure efficient data-flow control. Consequently, an enhanced router architecture is needed to achieve the requested QoS.

This paper proposes an internal router architecture, for on chip communication, implementing flow-control mechanism for congestion avoidance with QoS consideration. It describes the internal functions of this router for optimal output flit scheduling and its capability to apply per-class service for inbound flows. The paper focuses mainly on the description and performance analysis of two proposed schemes for data flow control that can be used with the proposed router architecture. The results shown in this paper prove that the application of these proposed schemes in NoC achieves an interesting enhancement in the measured end to end QoS. We carried out an extensive comparison of the proposed solutions with the existing schemes published in the literature to show that the proposed solution outperforms these, maintaining an interesting tradeoff with the hardware characteristics when designed with 45 nm integration technology.

1. Introduction

The communication aspect of Multi-Processor Systems-on-Chip (MP-SoC) is one of the biggest challenges in the new generation of embedded systems. A lot of active research is directed toward designing an efficient communication architecture for these systems. In depth, Networks-on-Chip (NoC) used to interconnect the multi-cores, are characterized by high-bandwidth links between the routers due to the high frequency

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of the chip. However, the area cost of the memory part of the integrated circuit strongly limits the memory capacity of the router, which limits its ability to absorb heavy traffic bursts. The lack of memory in these routers confronts the networks to the problem of congestion. It induces substantial flit losses and overhead delays that heavily affect the perceived quality of service at the application.

The efficient design of these systems requires to take into account and combine different constraints. In particular, embedded hardware constraints have to be considered simultaneously with networking constraints in order to evolve the NoC to meet the requirements of end-to-end QoS (e.g. end to end delay, jitter variation, number of lost flits, throughput at the reception level, etc). In this regard, data flow and congestion control mechanisms designed for computer networks-oriented routers are not applicable in our context.

Recently, very-large-scale integration (VLSI) technology has offered a flexible and powerful environment for the designers of digital circuits (Chen et al., 2009). Indeed, it allows maintaining a tradeoff between the complexity of used algorithms and the cost of the designed circuits. Additional tasks to manage QoS in NoC routers are, therefore, possible with relatively acceptable hardware overhead. With this consideration, the main challenge lies then, in the specification and implementation of an efficient scheme for congestion control applicable to on-chip communication.

High flit arrival rate in NoC routers requires an enhanced scheme for internal queuing of the incoming flits that helps to process and forward them according to their QoS constraints taking into account at the same time the router instant load. To achieve this goal, a per-flit management process should be implemented according to the importance of the payload data type of the transported flit.

The main contribution of this paper is, then, to propose a new architecture of NoC router with integrated mechanisms for congestion control. It presents two schemes for congestion control with respect to the end-to-end QoS requirements. The first proposed scheme is based on output buffering of flits before they are injected into the next hop that is experiencing congestion. The second proposed scheme, called feedback signaling mechanism, is a buffer-less approach based on the interaction between the source and router in congestion to notify the source to reduce its sending window size. The paper evaluates the efficiency of the proposed congestion control solutions for different traffic loads by comparing the performances of the two proposed schemes regarding QoS.

The remainder part of this paper is organized in the following sections. We first survey the main existing contributions in the area of congestion and data flow control in network on chip. We secondly, present the proposed router architecture and the proposed schemes for data-flow and congestion control. We will then focus on the evaluation of the flow-control mechanisms in terms of QoS and congestion control. Finally, we discuss the hardware characteristics of our proposed router before ending with a conclusion and directions for future work.

2. Overview of related work

NoC communication, which is characterized by high bandwidth, has recently become an active research area, mainly regarding the problems of data-flow control and congestion management. The main goal is to improve the efficiency of bandwidth allocation while avoiding router saturation. Traffic balancing based on a congestion-aware, adaptive routing process is an interesting approach to achieve load fairness (Wang et al., 2012). This solution often involves an exchange of load states and link utilization between neighbors, optimizing the routing process according to these exchanged data.

The authors in Lotfi-Kamran et al. (2010) studied a new solution for congestion avoidance based on dynamic XY routing (DyXY). In their approach, called Enhanced Dynamic XY (EDXY) routing, each router signals congestion to its neighbors through a two-bit bus. The presented solution keeps all data flows from trying to share the same path, consequently reducing data traffic congestion. Performance analysis of this solution has demonstrated good results for packet latency across these routers, outperforming the direct XY routing approach. However, this scheme did not address the problem of congestion as a general phenomenon, which might affect a network even with traffic distribution.

In Wang et al. (2013), a scheme using an energy- and buffer-aware adaptive routing algorithm (EBAR) was proposed to distribute thermal energy in a NoC. The main idea is to share data traffic for optimal thermal distribution across the NoC, while maintaining fair communication performance. For that purpose, the routing of flits is based on the thermal state of the next hop, avoiding high-temperature routers in the communications path. Thermal management is a critical problem in the design of integrated systems on chips (SoCs), but from a communications point of view, the proposed approach does not address congestion problems.

Congestion-awareness techniques based on signaling have been proposed as an efficient method to share locally the state of router buffers (Aci and Akay, 2010; Kaddachi et al., 2008; Daneshtalab et al., 2012). The intention is to avoid congested areas in the communications path. Applying this method requires broadcasting congestion information using extra buses or with additional data carried by the flits. We think that this method is interesting; however, we believe that it should be enhanced with the application of an adequate flow-control mechanism.

Ebrahimi et al. (2012) have studied a new algorithm for the routing process that uses local and non-local network information. The proposed scheme, called the Congestion Aware Trapezoid-Based Routing Algorithm (CATRA), defines a set of nodes that are likely to be involved in the data-communication path based on their congestion status. The congestion information is diffused through an extra bus that allows real-time updating without increasing traffic. The paper discussed the hardware implementation of this scheme, demonstrating that the additional cost to implement the proposed idea is reasonable in terms of circuit area and power consumption. While this approach seems attractive for NoC implementation, the paper did not show any enhancement to end-to-end QoS at the application level, which would be the main argument to justify its adoption.

An approach to flow control was proposed by Becker et al. (2012). The presented solution aims to control the input buffers occupation per data flow. The proposed scheme determines the credit allowed for each virtual channel based on performance observations. The authors demonstrated the efficiency of this approach, but they did not study its power consumption.