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ScienceDirect

Procedia Computer Science 45 (2015) 533 – 539

Procedia Computer Science

International Conference on Advanced Computing Technologies and Applications (ICACTA-2015)

A Theoretical analysis of Fibonacci coding techniques on On-chip Data Bus

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Abstract

As VLSI technology has scaled down towards the Deep Sub-micrometer (DSM) technology the crosstalk delay is flattering a great part of the total delay of a circuit. In addition, the escalating of cross-coupling capacitances among on-chip bus wires on the identical metal layer generates a situation where the delay of a wire is effectively relying on the electrical status of its adjacent wires. Therefore the data patterns on the on-chip data bus will affect the crosstalk delay. In this Paper, the performance of the Fibonacci coding techniques with respect to transition energy and crosstalk delay has been carried out and compared between them. The simulation results show that the NFF, RF and CRF coding technique offers on average ~50% energy savings and average ~30% delay reduction. So the entire system performance increases while the crosstalk delay reduces. Hence, these coding techniques increase the speed of the bus and/or diminish the total energy dissipation.

Peer-review under responsibility of scientific committee of International Conference on Advanced Computing Technologies and Applications (ICACTA-2015).

Keywords: Cross-coupling capacitance; DSM; On-chip bus; Crosstalk; Fibonacci number system.

1. Introduction

While VLSI technology has scaled down into the deep sub-micrometer (DSM) technology, novel challenges are surfacing to the VLSI circuit design engineers. The main key challenge is, the performance of bus based on-chip

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Peer-review under responsibility of scientific committee of International Conference on Advanced Computing Technologies and Applications (ICACTA-2015).
doi:10.1016/j.procs.2015.03.098

interconnects has become a bottleneck to the entire system performance. In high performance system like systems-on chip (SoCs), Multiprocessors and DSP processors the delay due to interconnects which constitute the on-chip data buses and global buses is dominant than the logic gate delay.

Crosstalk has become a main culprit for energy dissipation and crosstalk delay of on-chip data buses. Fig.1 shows a on-chip data bus capacitive model which is used for the analysis of crosstalk and energy dissipation. C_L is the *load capacitance* which includes the receiver gate capacitance and also the wire-to-substrate parasitic capacitance. C_I denotes the coupling capacitance occurring between neighbouring wires of the bus. In DSM technology, the space between on-chip bus wires is reduces, hence the C_I dominates the C_L i.e. load capacitance [4]. The interwire or coupling capacitance depends on the transitions occurring on the on-chip bus wires. The transitions are two types.

1) ***Self-transition:*** The transitions occurring on the same on-chip data bus wire.
2) ***Coupling transition:*** The transition occurring on the adjacent on-chip data bus wires.

The maximum speed of the signals on on-chip data bus is limited by the crosstalk and worst case crosstalk occurring between the adjacent wires. It has been shown that the performance of the on-chip data buses can be improved by controlling the amount of crosstalk occurring on the data bus [1, 2].

Numerous methods have been projected in literature to remove crosstalk transitions. Shielding technique (SHD) is proposed [3] to remove crosstalk transitions by placing a shield wire alternatively among wires of the on-chip data buses. As there is no transition on shield wires, the SHD method totally removes crosstalk transitions, hence the speed of the bus is improved around 50% but it requires twice the number of bus wires which results an increase of 100% area overhead.

One of the best techniques to improve the performance of the on-chip data bus is to encode the data pattern present on the bus to avoid the data transitions and data patterns in code word which generates the crosstalk [5, 7].

1) **Forbidden transition:** A transition from one codeword to a different codeword does not cause neighbouring wires to transition in opposing directions.
2) **Forbidden pattern:** The patterns “101” or “010” codewords are not visible in any one of the codeword.

Forbidden pattern coding (FPC) technique [5] prohibits 010 and 101 patterns from codewords, so crosstalk transitions are eliminated. It requires 52 wires for a 32-bit on-chip data bus.

To overcome these problems a novel method is given [7], which include the Forbidden Transition Free Crosstalk Avoidance Code. This method eliminates the existing problems and in this the Fibonacci number system is used for mapping scheme between the input dataword and Encoded dataword. In this paper, the performances of the 8-bit, 16-bit and 32-bit data buses are analyzed using Fibonacci coding techniques. This technique requires only 40 to 46 wires compared to SHD method which requires 63 wires for 32-bit data bus.

2. Cross-talk Classification

The data transition patterns on the data bus are used for classifying the crosstalk on on-chip data buses. The crosstalk patterns are classified as 0C, 1C, 2C, 3C, and 4C patterns as in [5], which are given in Table1.

The delay expression for the on-chip data bus capacitive model shown in Fig. 1 is given in equation (1) is in [1]. The delay T_j of the j^{th} wire is given in equation (1) as

$$T_j = abs\left(k.C_L.\Delta V_j + k.C_I.\Delta V_{j,j-1} + k.C_I.\Delta V_{j,j+1}\right) \quad (1)$$

3. Energy dissipation of On-chip data bus with crosstalk

The average bus energy dissipation is affected by crosstalk. The energy dissipation on the on-chip data bus is given in equation (2). The energy equation states that the total bus energy is obtained by summing up of the energy dissipation of every bus wire, which means energy dissipation depends on the transitions on the data bus. The total energy dissipation on on-chip data bus is given as