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ScienceDirect

Procedia Computer Science 86 (2016) 95 – 99

Procedia Computer Science

2016 International Electrical Engineering Congress, iEECON2016, 2-4 March 2016, Chiang Mai, Thailand

A low dropout voltage regulated bulk-driven CMOS current mirror

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Abstract

Novel bulk-driven current mirror (CM) and bulk-driven cascode CM are presented in this paper. Bulk-driven technique is employed to overcome a threshold voltage limitation. Proposed circuits operate at 1 V power supply. By using a negative feedback, high accuracy input and output transfer characteristic over wide current range is achieved. The proposed circuits are simulated using a 0.18 μm CMOS technology. The headroom voltage is 0.11 V for the proposed bulk driven CM and 0.16 V for the proposed bulk driven cascode CM.

Peer-review under responsibility of the Organizing Committee of iEECON2016

Keywords: Bulk-driven Technique; Current Mirror; Low Voltage

1. Introduction

Base on CMOS technology trend, it is necessary to scaling down supply voltage and power consumption while obtaining high performance. Current mirror is an essential building block of analog design. One major problem in designing a low voltage circuit is the threshold voltage because it does not scale down with transistor size. In order to overcome the threshold voltage limitation, a bulk-driven technique is employed[1,2]. Simple bulk-driven current mirror (CM)[1] and bulk-driven cascode CM[2] were introduced with limited input-output current matching and current range.

In gate-driven current mirrors, high accuracy current transfer over wide current range can be attained by regulating the drain voltage of transistor pair to the same value. This can be done via a negative feedback using a

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Peer-review under responsibility of the Organizing Committee of iEECON2016
doi:10.1016/j.procs.2016.05.024

loop amplifier[4]. This comes with a feature of output impedance enhancement. Due to its cascode structure, it is difficult to operate at a low supply voltage. However, this technique can be applied to the bulk-driven current mirror by regulating the bulk voltage to an appropriate value according to the input current. Thus a regulated bulk-driven CM requires low dropout voltage while obtaining high output impedance.

This work utilizes a standard 0.18 μm CMOS process. Theoretical analysis and simulation results are presented. Comparison of performance with conventional gate-driven CMs and bulk-driven CMs is also included.

2. The proposed bulk-driven current mirror

Simple bulk-driven CM[1] which has a nonlinear input-output current transfer was proposed. The reason of nonlinear current transfer is due to the fact that transistors are operated in triode region (by connecting the gate to V_{DD} for NMOS or V_{SS} for PMOS), hence a difference in drain-source voltage causes current mismatch. In order to enhance its current range, transistor pair must be in saturation region. This was done by connecting their gates to an appropriate value[5]. In case of bulk-driven cascode current mirror[2,3,5], the current mismatch still cannot be overcome. One solution is to force the transistors to operate in saturation region and selecting an appropriate gate bias voltage to achieve preferable current matching.

Both simple bulk-driven CM and cascode bulk-driven CM are not appropriate for a low voltage application because of low dynamic range and nonlinear current. Current mismatch occurred as a result of inequality of drain-source voltage at input and output side.

As previously explained, a higher dynamic range bulk-driven CM can be achieved by selecting an appropriate gate bias voltage. In order to expand the dynamic range, the gate voltage should be adjusted according to the input current. By using a negative feedback via a loop amplifier, the gate voltage is under controlled.

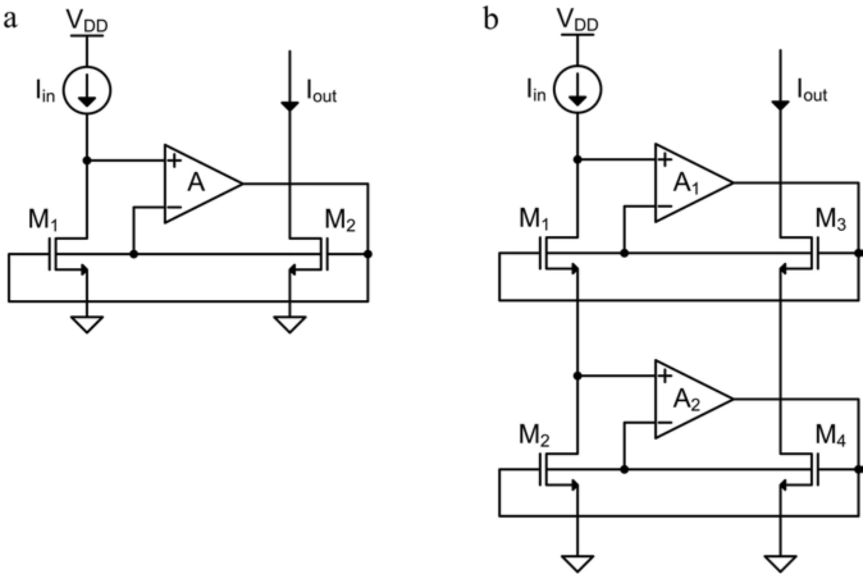

Fig. 1. (a) The proposed bulk-driven CM; (b) The proposed bulk-driven cascode CM

The proposed bulk-driven CM is shown in Fig. 1(a). It consists of transistor pair (M_1-M_2) along with a loop amplifier A. The gate voltages of both transistors are adjusted according to the input current by sensing the drain voltage of input transistor M_1 and bulk voltages of both transistors. Concerning the output transistor M_2, if the output voltage (drain of M_2) rises, the output current starts to increase. As a result, bulk of M_2 (also M_1) increases which in turn makes the gate voltage to decrease, the output current then decrease to the original value. Hence, output impedance is improved. However, the drain-source voltages of both transistors are unequal resulting in an input-output current mismatch.