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Modeling and Simulation of Junction Temperature Rise of GaN Devices for Class D Resonant Converters

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Abstract

Reliability of power electronic devices is related to their thermal performance. This paper presents the development of an electro-thermal model used to estimate junction temperature rise from self-heating effect in a GaN FET. Transient thermal impedances of the power device and the customized heat sink are extracted as a Foster thermal network before converting to a Cauer network to allow direct integration between multiple thermal networks. The proposed thermal impedance networks provide junction temperature information to the temperature-dependent SPICE model of the GaN FET so that self-heating effect is captured. The model is validated in SPICE simulation using a class D resonant converter as a case study. The results reveal the tendency of mismatch device temperature over a period of time posing a concern for the converter.
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Keywords: GaN FET, electro-thermal modeling, heat sink design, thermal management

1. Introduction

One of the most important factors that limit long-term reliability of power electronic devices is related to their thermal performance. Local dissipation of power devices and variation in ambient temperature over a long period of time will exert thermal cycle on the device assembly leading to thermal fatigue and package wear-out [1]. An

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enhancement-mode GaN FET has been introduced in a chip-scale Land Grid Array Package (LGA) and its thermal performance is improved over MOSFETs in conventional packages since dissipated heat can be conducted away from both side of the chip [2]. However, a small surface of the LGA package results in very high heat flux in the die; thus, design of heat sinking for such limited surface area becomes even more challenging in order to maintain power device temperatures within their limits. This paper presents the approach to develop a compact and accurate electro-thermal model of GaN FETs using lumped thermal impedances to include into standard SPICE models for more realistic simulation of the rise in device junction temperature, which could lead to the formation of hotspots near device channels and is a severe problem for high power GaN devices [3]. Using a class D resonant converter as a case study, a brief discussion on the simulation results, and conclusions drawn with recommended future work are presented.

2. GaN FET Electro-Thermal Model

In circuit simulation, an electro-thermal model provides a mean to estimate junction temperature response to power dissipation transients in power devices. In this study, a self-heating model of a GaN FET is developed based on the static-temperature model provided by the manufacturer [4]. To create dynamic electro-thermal models, it is required to update the junction temperature data in every time step. Hence, power dissipation in the FETs (P_D) is calculated in every cycle and coupled to the combined thermal networks to estimate the junction temperature rise. Then, temperature-dependent parameters are updated so that self-heating effect can be observed.

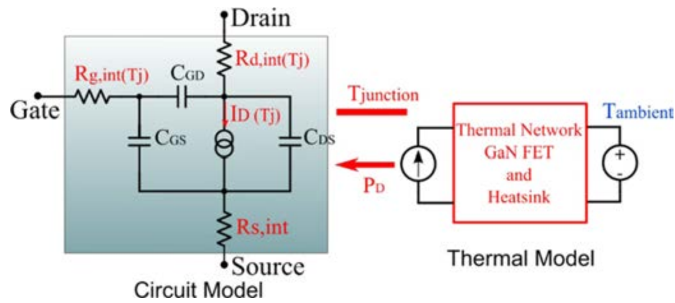

Fig. 1. GaN FET electro-thermal model

2.1. Extracted Thermal Impedance of GaN Power Device

The thermal path from chip to case of the GaN FET is considered as a one-dimensional heat flow problem. Thus, it is modeled by a simple transient thermal impedance (Z_{th}) as described by (1).

$$Z_{th}(t) = \frac{T_j(t) - T_{ref}}{P_D(t)} \quad (1)$$

where T_j is junction temperature, T_{ref} is case surface temperature, and P_D is dissipated loss of the power device.

The thermal circuit shown in Fig. 2 is in analogous to an electrical RC circuit and can be included in SPICE circuit simulations easily. The Cauer network in Fig. 2(a) is preferred; however, more often that the manufacturer provides thermal models using a Foster impedance network with no physical meaning (Fig. 2(b)) due to its simple curve fitting method. Therefore, a transformation to the Cauer model is required for our purpose.

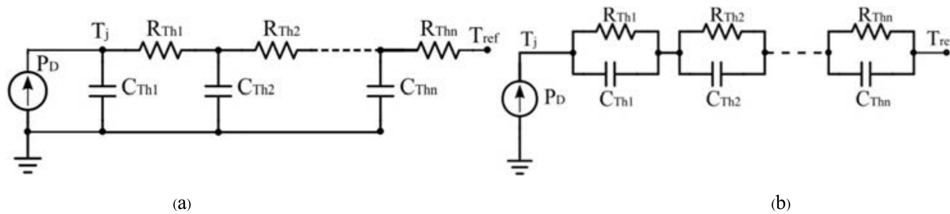

Fig. 2. Transient thermal impedance network (a) Cauer network (b) Foster network

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