Simulation Modelling Practice and Theory 29 (2012) 109–122

Contents lists available at SciVerse ScienceDirect

Simulation Modelling Practice and Theory

journal homepage: www.elsevier.com/locate/simpat

Optimization of IC encapsulation considering fluid/structure interaction using response surface methodology

C.Y. Khor *, M.Z. Abdullah

School of Mechanical Engineering, Universiti Sains Malaysia, Engineering Campus, 14300 Nibong Tebal, Penang, Malaysia

ARTICLE INFO

Article history:
Received 13 March 2012
Received in revised form 7 July 2012
Accepted 9 July 2012
Available online 3 September 2012

Keywords:
Integrated circuit (IC) encapsulation
Fluid structure interaction (FSI)
Response surface methodology (RSM)
Central composite design (CCD)

ABSTRACT

Optimized design of the integrated circuit (IC) package gives better IC encapsulation process and minimizes the stress concentration and deformation of the IC structures. The physical and process parameters (i.e., pressure inlet, solder bump standoff height, chip thickness, gap-wise between chips, and mould and filled time) were optimized via response surface methodology using central composite design (CCD) to minimize the stress concentration of chip and solder bump, chip deformation, and void in package during the IC encapsulation process. The optimization of the moulded IC encapsulation is carried out by considering the fluid/structure interaction (FSI) aspects. The optimum empirical models were tested and well confirmed with the simulation results. The optimum design of the IC package (20 mm × 20 mm) with perimeter solder bump arrangement for both physical and process parameters was characterized by 150 μm of solder bump standoff height, 250 μm of chip thickness, and 50.43 μm of gap-wise at the inlet condition of 3.43 MPa.

1. Introduction

Integrated circuit (IC) package design, material selection, and process parameters are significant factors in package reliability. The physical characteristic of the IC package, such as package size, solder bump count, solder bump shape, diameter, arrangement, standoff height, silicon chip thickness, mould gap-wise, and inlet/outlet design, can influence the package reliability in subsequent manufacturing processes. In the IC encapsulation process, the feeding of epoxy-moulding compound into a cavity causes the fluid–structures interaction (FSI). Optimal process setting and IC design can minimize the deformation and fluid-induced stress on the structures (e.g., silicon chip, solder bump, wire bonding, paddle, and lead-frame). Moreover, a properly controlled moulding process yields lower void or air traps in the IC package.

Several methods have been utilized to optimize the IC packaging, including the Taguchi method [1], artificial neural networks (ANNs) [2], genetic algorithm (GA) [3], neuro-fuzzy genetic algorithm [4], and response surface methodology (RSM) [5]. RSM had been utilized for the investigation of the ball grid array (BGA) package by van Driel et al. [5] using the three-dimensional finite element (3D-FE) virtual prototyping. Besides, the optimal process parameter setting of the thin quad flat package (TQFP) [4] and plastic dual-inline package (PDIP) [6] moulding process was achieved through the neuro-fuzzy-GA approach and Taguchi method. Chen et al. [7] used Taguchi method to optimize the design of plastic quad flat packages (PQFP) in the curing process. In microelectronic industry, the optimization of the IC encapsulation process with the consideration of fluid–structure interaction (FSI) is significant [8]. The understandings of interactive influences between various parameters are crucial to eliminate the unintended IC defects. The optimized parameters can be achieved using RSM, which

* Corresponding author. Tel.: +60 195637283.
E-mail address: cykhor_1985@hotmail.com (C.Y. Khor).

1569-190X/$ - see front matter © 2012 Elsevier B.V. All rights reserved.
http://dx.doi.org/10.1016/j.simpat.2012.07.003

Nomenclature

A_1, A_2	pre-exponential factors (1/s)
B	exponential-fitted constant (Pa s)
C_1,C_2	fitting constant (–)
C_P	specific heat (J/kg K)
E_1,E_2	activation energies (K)
E	elastic modulus (GPa)
F	front advancement parameter (–)
k_1, k_2	rate parameters described by an Arrhenius temperature dependency (1/s)
m_1, m_2	constants for the reaction order (–)
n	power law index (–)
p	pressure (Pa)
T	temperature (K)
t	time (s)
T_b	temperature-fitted constant (K)
u	fluid velocity component in x-direction (mm/s)
v	fluid velocity component in y-direction (mm/s)
w	fluid velocity component in z-direction (mm/s)
x, y, z	Cartesian coordinates (–)

Greek letters

α	conversion of reaction (–)
α_{gel}	degree of cure at gel (–)
ΔH	exothermic heat of polymerization (J//kg)
η	viscosity (Pa s)
η_0	zero shear rate viscosity (Pa s)
ρ	density (kg/m^3)
ρ_s	solid density (kg/m^3)
τ	shear stress (Pa)
$\dot{\gamma}$	shear rate (1/s)
τ^*	parameter that describes the transition region between zero shear rates and the power law region of the viscosity curve (Pa)
v	Poisson ratio (–)

can reduce the simulation runs and efficient for multi-target optimization [5]. Thus, the investigation using RSM with central composite design (CCD) is considered for a moulded IC packaging in the current study.

In this study, the IC encapsulation process is simulated using FLUENT 6.3.26, ABAQUS 6.9, and MpCCI [8] for FSI analysis. The Castro–Macosko model with curing effect describes the epoxy-moulding compound (EMC) behaviour by the appropriate user-defined functions (UDFs) in FLUENT analysis. The EMC flow front is tracked using the volume of fluid (VOF) model while the forces induced during encapsulation (FLUENT) are transferred to ABAQUS for simultaneous structural analysis. Moreover, this virtual modelling technique [8] for the IC package optimization study should provide reliable predictions and optimize the combination of process and physical parameters in the IC encapsulation. This study examined the individual and interactive influences of factors in IC package design on the minimization of stress concentration on chip and solder bump, chip deformation, void in the package, and filled time.

2. Problem description

In the IC encapsulation process, interaction between the epoxy-moulding compound (EMC) and IC structures yields the undesired deformation and stress concentration. This phenomenon is widely reported in the IC package with wire bonding. The trend towards the miniaturization of IC packages presents a challenge to the engineer and package designer. Defects such as structure deformation, high stress concentration, and void formation during encapsulation reduce the IC package reliability. Various sizes of IC package are designed for diverse applications in the microelectronic industry. Different IC package dimensions may have different optimized values for each design. In the current study, an IC package with dimensions of 20 mm $\times$ 20 mm and perimeter type of solder bump arrangement is considered for the optimization by focusing on the design and process parameters. Fig. 1 illustrates the moulded IC package or moulded underfill package, where the underfill and encapsulation processes are taken in one step. The physical dimensions of the IC package are summarized in Table 1. The application of linear solder bump shape [9] yielded lower stress concentration; thereby, this solder shape is considered in the package design. In the RSM analysis, the factors are selected according to their influences in terms of deformation, stress