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Research paper

SEU mitigation exploratory tests in a ITER related FPGA

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ABSTRACT

Data acquisition hardware of ITER diagnostics if located in the port cells of the tokamak, as an example, will be irradiated with neutrons during the fusion reactor operation. Due to this reason the majority of the hardware containing Field Programmable Gate Arrays (FPGA) will be placed after the ITER bio-shield, such as the cubicles instrumentation room. Nevertheless, it is worth to explore real-time mitigation of soft-errors caused by neutrons radiation in ITER related FPGAs. A Virtex-6 FPGA from Xilinx (XC6VLX365T-1FFG1156C) is used on the ATCA-IO-PROCESSOR board, included in the ITER Catalog of Instrumentation & Control (I & C) products – Fast Controllers. The Virtex-6 is a re-programmable logic device where the configuration is stored in Static RAM (SRAM), the functional data is stored in dedicated Block RAM (BRAM) and the functional state logic in Flip-Flops. Single Event Upsets (SEU) due to the ionizing radiation of neutrons cause soft errors, unintended changes (bit-flips) of the logic values stored in the state elements of the FPGA. Real-time SEU monitoring and soft errors repairing, when possible, were explored in this work. An FPGA built-in Soft Error Mitigation (SEM) controller detects and corrects soft errors in the FPGA Configuration Memory (CM). BRAM based SEU sensors with Error Correction Code (ECC) detect and repair the respective BRAM contents. Real-time mitigation of SEU can increase reliability and availability of data acquisition hardware for nuclear applications. The results of the tests performed using the SEM controller and the SEU sensors are presented for a Virtex-6 FPGA (XC6VLX240T-1FFG1156C) when irradiated with neutrons from the Portuguese Research Reactor (RPI), a 1 MW nuclear fission reactor, operated by IST in the neighborhood of Lisbon. Results show that the proposed SEU mitigation technique is able to repair the majority of the detected SEU soft-errors in the FPGA memory.

1. Introduction

A nuclear fusion tokamak [1] like ITER [2] will be a reactor generating neutrons during operation. For instance, in ITER port cells the expected neutrons (n) energies will be between 14 MeV and 100 keV, with fluxes between 10^2 n/cm^2/s and 10^5 n/cm^2/s respectively [3]. Data acquisition hardware normally includes Field Programmable Gate Arrays (FPGA) for signal processing, among other tasks. As an example, the ITER Catalog of Instrumentation & Control (I & C) products – Fast Controllers [4] contains instrumentation based on FPGAs. The non-destructive effects of the ionizing radiation due to neutrons in those devices can be partially mitigated. The FPGA reliability and availability in neutron environments can be increased with real-time mitigation of some of the radiation effects.

A Virtex-6 FPGA (XC6VLX365T-1FFG1156C) from Xilinx is used on the board ref. ATCA-IO-PROCESSOR [5] of the ITER fast controllers catalog. To perform the tests of the FPGA, a Xilinx development kit (ML605) [6] was used since it has a lower cost relatively to the ATCA-IO-PROCESSOR board. The development kit contains an FPGA of the same family (XC6VLX240T-1FFG1156C) allowing cheaper preliminary tests in case of board damage and activation due to the neutron radiation.

The Virtex-6 FPGA is a re-programmable logic device where the configuration is stored in Static RAM (SRAM), the functional data is stored in dedicated Block RAM (BRAM) and the functional state logic in Flip-Flops. Neutron radiation can induce Single Event Upsets (SEU), also known as soft errors or bit-flips, in the state elements of the FPGA. Neutron radiation can also cause permanent damage to FPGAs but it is out of the scope of this work. In the carried

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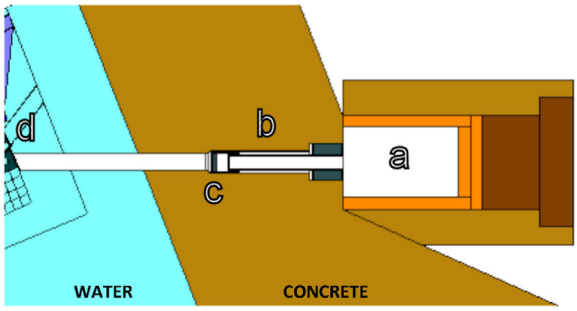

Fig. 1. RPI fast neutrons irradiation facility E4, showing: (a) irradiation chamber at the exit of neutron beam tube; (b) extension inside the tube; (c) neutron and gamma filter; and (d) periphery of the fission reactor core inside the water cooling/shielding pool.

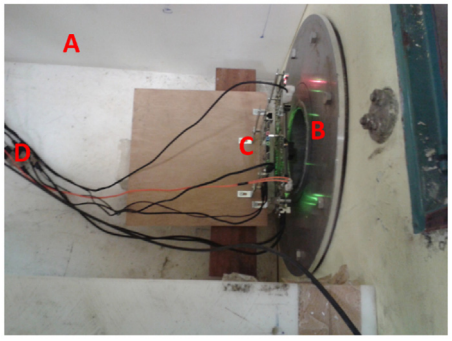

Fig. 3. Irradiation chamber, showing: (A) chamber inside; (B) exit of the fast neutron beam tube E4; (C) target FPGA assembled on a ML605 Xilinx board and wooden support; and (D) cabling connecting the external experimental setup equipment.

out experimentations the real-time SEU detection (and respective errors correction) in the FPGA configuration and BRAM memories were tested, using a Soft Error Mitigation (SEM) controller (an available hard IP core in the FPGA device) and BRAM based SEU sensors with hard Error Correction Code (ECC).

2. Experimental setup

The tests have been performed on the Portuguese Research Reactor (RPI), a 1 MW nuclear fission reactor operated by Instituto Superior Técnico (IST) of the University of Lisbon (UL), in the neighborhood of Lisbon. The reactor irradiation facility used was the fast neutron beam tube E4 and respective chamber [7]. Fig. 1 shows the layout of the RPI fast neutrons irradiation facility E4.

As the tests needed to be scheduled accordingly with the agenda availability of RPI fast neutrons irradiation facility, the experimental setup was planned to be monitored and operated remotely using the Internet. In this way numerous journeys between Instituto de Plasmas e Fusão Nuclear (IPFN) and RPI site have been avoided. The AC power supplies of the experimental equipment were independently ON/OFF controlled allowing recovering from possible failures, due to e.g., PCs or FPGA board crashes.

The experimental setup, Fig. 2, comprises an irradiation chamber (Fig. 3), a Xilinx ML605 board with the FPGA device (XC6VLX240T-1FFG1156C) to test, communications and power cabling (electrical and optical), an ON/OFF controller (APC AP7920) for the AC power supplies of the equipment, an Ethernet switch and two PCs.

One of the PCs (Windows OS) was used for the FPGA programming and also to run the software needed for monitoring the SEU tests in the FPGA Configuration Memory (CM) and in the BRAM. The other PC (Linux OS) was running the ITER data acquisition software of the ATCA-IO-PROCESSOR board [8].

The standard EIA-232 communications between the PC and the UART of the FPGA have been used for the CM and BRAM SEU tests.

FPGA programming and configuration read-backs were done through the Xilinx JTAG tool.

Optical PCI Express communications between the ITER data acquisition PC and the FPGA were used to emulate the Advanced Telecommunications Computing Architecture (ATCA) based infrastructure, which normally hosts the ATCA-IO-PROCESSOR board [9,10].

3. Firmware

Fig. 4 illustrates the FPGA firmware and respective board interfaces used. The firmware implemented for the tests includes three main blocks: The built-in SEM controller, for SEU detection and mitigation in the configuration memory; The proposed BRAM based sensors, for SEU detection and mitigation in the BRAM memory; The ITER data acquisition logic.

The SEM controller and the implemented BRAM based SEU sensors do not operate on soft errors in distributed memory or flip-flops. Soft-error mitigation in these memory resources need to be addressed by the user logic through preventive measures such as

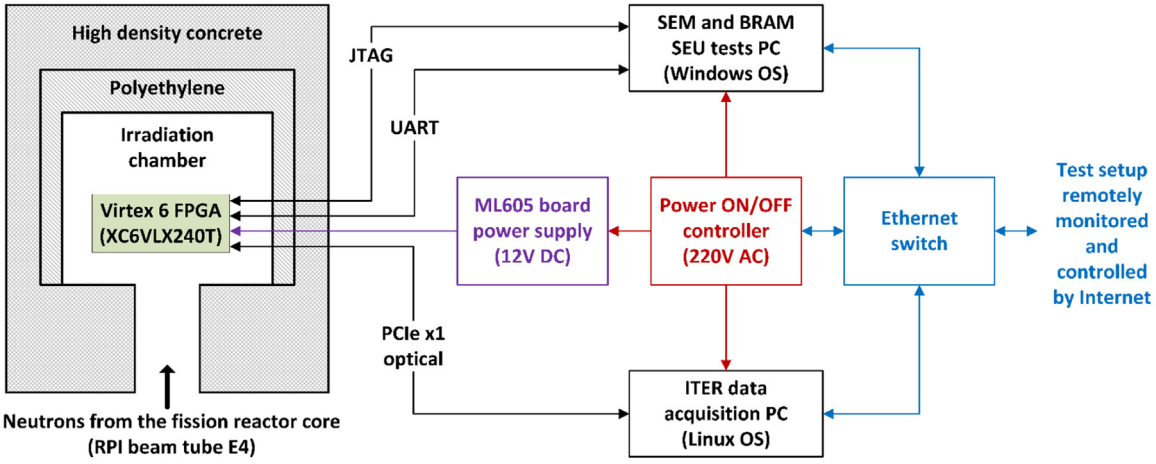

Fig. 2. Experimental setup for the FPGA irradiation tests with neutrons.