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An approach to build cycle accurate full system VLIW simulation platform

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ABSTRACT

Very long instruction word (VLIW) architecture is widely used in the design of digital signal processors (DSPs) and application-specific processors because of its hardware simplicity and high efficiency. Some heterogeneous systems also use VLIW style accelerators to achieve high computing performance and power efficiency. However, there are few widely accepted simulators that can cycle-accurately model a VLIW architecture or simulate the entire heterogeneous system with VLIW accelerators. In this paper we present an approach to build cycle accurate full system VLIW simulation platform. The basic idea is to analyze Petri Nets modeling used in the traditional cycle accurate simulation and adjust it to match VLIW architecture. The adjustments reconstruct and optimize the colored token, the place and the arc in Petri Nets in order to adapt it with VLIW characteristics. According to our approach and based on the InOrder simulator in the open source simulator framework Gem5, we build a heterogeneous multicore full system simulator for the MaPU (Mathematical Processor Unit) chip, which is composed by a functional accurate ARM simulator and a cycle accurate accelerator simulator. To evaluate the performance and accuracy of our simulator 'Gem5-MaPU', we compare the results of a set of DSP benchmarks executed by both the simulator and the RTL model. The result shows our simulator is about 1000 times faster than the RTL model while the cycle error is reduced to less than 5%. With high accuracy rate and good accelerating ratio over RTL simulation, the cycle accurate simulator turns out to be an efficient and flexible tool for VLIW related architectures' study and development, such as the hardware-software co-design and performance evaluation, etc.

1. Introduction

Very long instruction word (VLIW) architecture has been studied for several decades. A VLIW machine has long machine instructions, an orthogonal instruction set and a high degree of parallelism [1]. Compared with general purpose processor architectures like complex instruction set computing (CISC) and reduced instruction set computer (RISC) which use complex superscalar design, VLIW has unique advantages. This architecture uses simple control logic and structured hardware design to exploit instruction level parallelism (ILP), achieving high computing performance as well as reasonable power efficiency [2]. These features make it quite successful in the digital signal processing (DSP) and application-specific integrated circuit (ASIC) design areas, for applications like digital audio/video signal processing, pattern recognition and cellphone commu-

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nication, etc. A typical example is Texas Instruments' VelociTI architecture DSPs such as the TMS32OC6s family [3]. VLIW architecture is also used in building GPU. The well-known vendor AMD adopts VLIW structure to build its GPU products and there has been many research studying them, such as [4–6].

However, VLIW architecture does have some restrictions and deficiency. For many applications where the algorithms are not so regular or structured, VLIW processors would be less efficient and waste a lot of computing resource. Because of that, a common way is using VLIW accelerator to build heterogeneous computing systems. For example, mobile cellphones use VLIW DSP cores like TI's TMS320C6x and ADI's Tiger-SHARC to meet communication and power efficiency requirements [7,8]. Many researches use CPU-GPU architecture to accelerate linear algebra algorithms and dense matrix computation [9–11]. Heterogeneous systems take advantage of multiple architectures, and the booming of these computing systems extends the usage of VLIW architecture greatly.

VLIW architecture is often used in the development of DSP, ASIC, and some other power sensitive situations. Usually these chip developments have long cycle and high cost, making the help of software simulators very important and necessary. Simulation is very helpful both in manufacturing and in academic studies [12]. With the help of software simulators, fast and low-cost analysis of systems is available. A good simulator gives help during all the time of chip development. It helps comparing alternative designs, supporting software–hardware co-designs and shorting the time to market, analyzing system performance and finding bottlenecks. For fast product development, precise and flexible simulators are very important.

Instruction set simulator (ISS) is commonly used in hardware simulation. ISS supplies software environment which reads microprocessor instructions and simulates the execution of hardware [13]. Usually ISS provides more information than real hardware, as it imitates the function of hardware and generates related results such as memory and register value, providing easier and more detailed way to observe these information. There are basically two kinds of ISS: the instruction accurate ones and the cycle accurate ones. Generally the instruction accurate simulators are fast and mainly used in developing software and tracing function-related information. While the cycle accurate ones are slower but they give much more detailed simulation of target systems. For some purposes like software performance estimation and real-time system analysis, cycle accurate simulation is necessary. There are many general purpose simulators, including SimpleScalar [14,15], SimOS [16], Gem5 [17], and IBM's Mambo, AMD's SimNow, etc. Many of those commercial or open-source simulators support multiple simulation models and different target processors.

However, few cycle-accurate simulators support the simulation of VLIW processors. Most of these widely used simulators such as SimpleScalar and Gem5 gives the modeling of many kinds of superscalar architectures like x86, MIPS, Spark, etc. Except for some specific VLIW simulators given to describe certain commercial products such as TI's DSP chips [18], most of other related researches and simulators only give instruction-accurate modeling and simulation, such as Simple-VLIW [19,20], or educational purpose researches like the VLIW-DLX simulator [21]. Some simulators provide function accurate simulating to estimate cycle-accurate information. None of them meets the requirements of the MaPU [22], which has the high performance accelerator consists of two types of heterogeneous VLIW units with precisely cycle-accurate programming model. The MaPU's high performance VLIW accelerator depends on a specially designed precise cycle-accurate pipeline to achieve all kinds of algorithms, giving quite a challenge to its software simulator on cycle accuracy and simulating speed.

Petri Nets are perfectly suitable to describe processor architecture and its running behavior. And there has been a lot of related research adapting Petri Nets or extending their features for all kinds of simulation purposes, such as for pipeline modeling [23], and for dynamic systems [24]. In this paper, we present an approach to build cycle accurate VLIW simulator based on open source simulator Gem5. The main contribution of this paper is to analyze the Petri Nets of Gem5 simulator, figuring out the features that don't match VLIW architecture and adjust the model to build VLIW simulation engine. Multi-pipeline model is also supported, to meet the requirement of simulating the whole MaPU's heterogeneous architecture.

The rest of the paper is organized as follows. Section 2 describes some basic concepts of Petri Nets, and the optimizations for Petri Nets made by Gem5 in the InOrderCPU model. Section 3 analyzes the problems of InOrderCPU model when it comes to VLIW architecture, and introduces our approach and modifications. Section 4 describes some key points of our simulator product, mainly about some modules' design and consideration. Section 5 shows the simulation results on a set of DSP benchmarks, analyzing simulating accuracy and speed. In the last, Section 6 summarizes the paper and describes the future work.

2. Petri Nets and InOrderCPU engine

2.1. Basic concept of Petri Nets

Petri Nets [23,25] have been proposed as an important mathematical tool for hardware systems modeling by Misunas [26], Ramchandani [27], Agerwala [28], etc. Events are key elements of a Petri Net model. There are a set of possible events in Petri Net model of hardware systems. Each event has pre-conditions and post-conditions. The occurrence of an event relies on its pre-conditions to be true and it drives its post-condition events to occur. The basic idea of describing a hardware system with Petri Nets is to enumerate all the events and define the pre and post conditions of them.

The elements of Petri Nets include place (circle node typically drawn as circles or hexagons), transition (square node typically drawn as lines or boxes), arc (directed arc between place and transition) and token (static object in place, possibly moving from one place to another). In CPU modeling area these elements stand for certain entities. Token is the abstraction of the carrier of information between parallel function modules and it usually stands for instruction, resource requestion or