

# Common-mode voltage reduction for space vector modulated three- to five-phase indirect matrix converter



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## ABSTRACT

All available Pulse Width Modulation (PWM) techniques employed to different Matrix Converter (MC) topologies generally generate switching Common-Mode Voltage (CMV), which introduces numerous operational concerns in electric drives. Although a body of research for the three-phase case has been undertaken to either reduce or eliminate CMV, corresponding discussions for multiphase MC remain scarce. Interestingly enough, the three- to five-phase ( $3 \times 5$ ) Indirect MC (IMC) is a potential converter topology for five-phase based high power motor drives. In this paper, the different available switching states of a  $3 \times 5$  IMC are classified based on their corresponding CMV levels. Accordingly, two different Space Vector Modulation (SVM) techniques are proposed, which can successfully reduce the peak CMV by 28% and 48%, respectively, when compared with the conventional modulation strategy, while the same maximum Voltage Transfer Ratio (VTR) is preserved. Although the 28% reduction has been alternatively achieved in literature based on carrier-based PWM, the 48% reduction attained in this study represents the maximum achievable reduction for this MC topology. The main concept is firstly introduced; then, both simulations and experiments are used to validate the proposed schemes.

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## 1. Introduction

MATRIX-CONVERTERS (MCs) are commonly proposed for direct ac-to-ac power conversion systems to convert an  $m$ -phase supply into a controllable  $n$ -phase output [1]. The main interest in this topology lies in its constructional and operational merits over similar conversion systems [2,3]. As indicated in the literature, the MCs are shown attractive in special applications, such as electric drive systems, renewable energy systems, aircrafts, and variable-speed diesel-generation systems [4,5].

There are two main topologies for MCs, namely, Direct MC (DMC) and Indirect MC (IMC) [6]. The DMC contains a matrix of bidirectional switches that interconnects each input phase with an output phase. On the other hand, the IMC consists of a bidirectional current controlled rectifier followed by a standard two-level Voltage Source Inverter (VSI). Although the two topologies are functionally equivalent [6,7], the IMC offers a reduced number of

switching devices for systems with a high phase order. Besides, it offers a simpler commutation technique over DMC [2]. From this standpoint, the IMC has received more attention and some innovative topologies with a reduced switch count, namely, sparse, very sparse and ultra-sparse MCs, are presented in [8]. The Z-source IMC is also proposed to improve the achievable voltage gain by inserting an X-shape impedance network between the rectifier and the inverter stages [9]. In order to improve converter output waveforms, a three-level neutral point converter was also proposed in the output-stage [10].

Recently, the multiphase drive systems are gaining much interest over three-phase counterparts, especially in high power safety-critical applications [1,11,12]. Although standard VSIs are commonly employed in such drive systems, the  $3 \times n$  phase MC represents a promising potential alternative topology to get rid of the bulky storage elements [13].

In the literature, modulation techniques based on either Carrier-Based PWM (CBPWM) or Space Vector Modulation (SVM) strategies [2,3,13,14] have been proposed to control the  $3 \times 5$  MC in both linear and over modulation modes. However, the PWM nature of the output waveform generates a series of spike-like Common Mode Voltage (CMV) with high frequency, which causes

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several serious problems to motor drive-systems [15]. The research studies on CMV reduction/elimination for the  $3 \times 3$  MC are relatively mature [16–18]. These studies have been applied to both DMC and IMC. However, similar discussions for multiphase systems were mostly limited to CMV reduction/elimination in multiphase VSIs [19–22]. Some recent papers investigated the reduction of CMV in  $3 \times 5$  MC [23–26] and  $3 \times 7$  MC [27] systems. The strategy proposed in [23] aimed to eliminate the CMV using dual  $3 \times 5$  DMC feeding an induction machine with an open-end winding. In [24], an approximate reduction of 18% in the generated CMV from a  $3 \times 5$  DMC is obtained by operating the converter in the over modulation operating mode using SVM algorithm. However, the output voltage and current waveforms experienced a notable distortion. The modulation technique proposed in [25] reduces the peak CMV of a  $3 \times 5$  IMC by 13.4% by selecting only one zero vector in each sector of the five-phase inverter stage. This method also reduces the converter switching actions. Finally, a CBPWM based on SVM algorithm of a  $3 \times 5$  IMC is proposed in [26] to reduce the peak CMV by 28% through the suitable selection and distribution of the zero vectors in both the rectifier and inverter stages. To the best of the authors' knowledge, none of the provided techniques was able to minimize the CMV of a  $3 \times 5$  MC below the mentioned levels.

This paper aims to present a thorough study to the generated CMV levels by different switching vectors of a  $3 \times 5$  IMC, and proposes two CMV reduction schemes based on SVM. The proposed schemes are able to reduce the peak CMV by 28% and 48% respectively while the same Voltage Transfer Ratio (VTR) is maintained. In order to validate the proposed CMV reduction schemes, simulation and experimental results for a five-phase inductive load are introduced.

## 2. Three- to-five-phase IMC and CMV analysis

### 2.1. Converter topology and space vector modeling

The power circuit topology of a  $3 \times 5$  IMC is shown in Fig. 1. It consists of a three-phase rectifier followed by a five-phase inverter without any interconnecting dc-link reactive elements. The rectifier consists of six bidirectional switches ( $S_1$ – $S_6$ ), while the inverter has five legs with ten unidirectional switches ( $S_7$ – $S_{16}$ ). The impedance  $Z_L$  represents the leakage impedance between the neutral point of the five-phase load and the supply ground point. The input filter in the configuration is usually used to attenuate the supply current switching harmonics.

The operational principle of this topology, based on space vector theory, is given in [2]. The input supply voltages and the desired five-phase output voltages are both assumed balanced and sinusoidal, as given by (1) and (2).

$$v_{A,B,C} = \hat{V}_i \cos(\omega_i t - 2\pi k/3), \quad k = 0, 1, 2 \quad (1)$$

$$v_{a,b,c,d,e} = \hat{V}_o \cos(\omega_o t - 2\pi j/5), \quad j = 0, 1, 2, 3, 4 \quad (2)$$

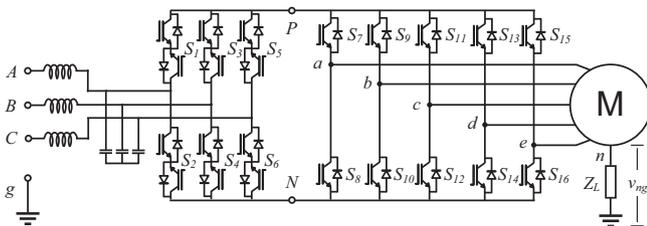


Fig. 1. Power circuit topology of the  $3 \times 5$  IMC.

where  $v_{A,B,C}$  and  $v_{a,b,c,d,e}$  are the instantaneous voltages,  $\hat{V}_i$  and  $\hat{V}_o$  are the peak voltages, and  $\omega_i$  and  $\omega_o$  are the input and output angular frequencies respectively.

The corresponding space vector modeling of the rectifier and the inverter stages is shown in Fig. 2. The space vector plane of the rectifier is composed of six active current vectors with a magnitude of  $2I_{dc}/\sqrt{3}$  and three zero (null) vectors. Each active vector represents a case where two input phases are connected to the fictitious dc-link. However, each zero vector yields a short-circuited dc-link. Fig. 2(b) and (c) shows the available space vectors of the five-phase inverter stage mapped to the two decoupled  $\alpha$ - $\beta$  and  $x$ - $y$  subspaces. All active voltage vectors can be classified according to their magnitudes to small ( $V_S = 4/5 \cos(2\pi/5)V_{dc}$ ), medium ( $V_M = 2/5V_{dc}$ ), and large ( $V_L = 4/5 \cos(\pi/5)V_{dc}$ ) voltage vectors [3].

### 2.2. Common mode voltage analysis of $3 \times 5$ IMC

The common mode voltage of a  $3 \times 5$  MC is defined as the potential difference between the neutral point of the five-phase load and the ground point of the three-phase supply. Similar to the  $3 \times 3$  MC [16–18], the CMV expression,  $v_{cm}$ , for the  $3 \times 5$  MC is given by;

$$v_{cm} = 1/5(v_{ao} + v_{bo} + v_{co} + v_{do} + v_{eo}) \quad (3)$$

It is clear that the CMV value depends typically on the five-phase output voltages obtained from the available 32 voltage vectors ( $V_0 - V_{31}$ ) of the inverter-stage. This stage is fed from the fictitious dc-link voltage,  $V_{pn}$ , which is decided based on the selected input rectifier current active vector. Therefore, the CMV is represented by a combination of the switching vectors of the inverter and rectifier stages, as given by (4) and (5).

$$v_{cm} = \frac{1}{5} \left\{ v_p \sum_{k=1}^5 S_{2k+5} + v_n \sum_{l=1}^5 S_{2l+6} \right\} \quad (4)$$

where

$$\begin{aligned} v_p &= S_1 v_A + S_3 v_B + S_5 v_C \\ v_n &= S_2 v_A + S_4 v_B + S_6 v_C \end{aligned} \quad (5)$$

It can be noted that the generated CMV in a five-phase case will have different voltage levels due to the relatively large number of voltage vectors in the five-phase case. For example, the active switching vector  $V_{24}$  '11000' of the inverter-stage generates a CMV of  $(2v_p + 3v_n)/5$ . If the reference input current is located in sector 1,  $S_1$  will be ON while  $S_4$  and  $S_6$  are modulated. Hence,  $v_p = v_A$  and  $v_n = v_B$  or  $v_C$ . This results in a peak CMV ranging from  $-\sqrt{3}\hat{V}_i/10$  to  $\sqrt{3}\hat{V}_i/5$ . While, if the reference input current is located in sector 2, the CMV will range from  $-3\sqrt{3}\hat{V}_i/10$  to  $-3\sqrt{3}\hat{V}_i/10$ . Thereby, the peak CMV generated  $-\sqrt{3}\hat{V}_i/10$  from the IMC due to switching vector  $V_{24}$  will be  $3\sqrt{3}\hat{V}_i/10$ .

The CMV magnitude corresponding to all available switching states is given in Table 1. Fig. 3 shows the envelope of the generated CMV due to both inverter and rectifier switching states. It can be noted from Fig. 3 and Table 1 that the CMV generated by the  $3 \times 5$  IMC has thirteen levels ( $0, \pm\sqrt{3}\hat{V}_i/10, \pm\sqrt{3}\hat{V}_i/5, \pm 3\sqrt{3}\hat{V}_i/10, \pm\sqrt{13}\hat{V}_i/5, \pm\sqrt{3}\hat{V}_i/2$  and  $\pm\hat{V}_i$ ). However, the levels of the peak CMV due to the inverter switching vector groups 1, 2 and 3 are only six ( $\pm 3\sqrt{3}\hat{V}_i/10, \pm\sqrt{13}\hat{V}_i/5$  and  $\pm\hat{V}_i$ ). Applying zero vectors ( $V_0$  and  $V_{31}$ ) will maximize the CMV. Therefore, by avoiding the zero vectors (vectors of group 1), CMV can be simply reduced, which yields a 28% reduction in the peak CMV. Employing only the switching vectors of group-3 will reduce the peak CMV by about 48% when compared with a conventional SVM scheme.

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