Electrical Power and Energy Systems 91 (2017) 117–120

Contents lists available at ScienceDirect

Electrical Power and Energy Systems

journal homepage: www.elsevier.com/locate/ijepes

Controllable electronic transformer based on the resonance structure with switching capacitor for low-rise buildings residential area power supply stabilization systems

L.G. Zotov [a], V.P. Razinkin [a], V.V. Atuchin [b,c,d,e,f,*]

[a] Department of Radio Engineering and Electronics, Novosibirsk State Technical University, Novosibirsk 630073, Russia
[b] Laboratory of Optical Materials and Structures, Institute of Semiconductor Physics, SB RAS, Novosibirsk 630090, Russia
[c] Functional Electronics Laboratory, Tomsk State University, Tomsk 634050, Russia
[d] Laboratory of Semiconductor and Dielectric Materials, Novosibirsk State University, Novosibirsk 630090, Russia
[e] Institute of Chemistry, Tyumen State University, Tyumen 525003, Russia
[f] Laboratory of Single Crystal Growth, South Ural State University, Chelyabinsk 454080, Russia

ARTICLE INFO

Article history:
Received 25 March 2016
Received in revised form 8 February 2017
Accepted 6 March 2017

Keywords:
Resonance structure with switching capacitor
Controllable electronic transformer
Bidirectional transistor switch
Pulse-width regulation

ABSTRACT

Based on a resonance structure with switching capacitor, a simple power circuit of high frequency controllable electronic supply line transformer having improved mass-size parameters and overvoltage protection of its transistor switches is considered. Analysis of its operation, formulae for calculation of power elements, regulating and load characteristics are presented.

1. Introduction

Intelligent electrical power distribution systems (smart grid) are based on the control by telecommunication and digital channels using operational information on the energy production and optimal electric power consumption. The systems provide higher efficiency and reliability, improve economic parameters and increase the tolerance of energy generation and distribution, including the peak power periods. The transmission and distribution system delivers electricity from the generating site to commercial and industrial facilities, and residential data processing and power control are the key elements of the smart grids [1–6]. The main quality indicators for low-rise buildings residential area power supply systems are low mass, small size, high efficiency factor (EF) and stability of AC supply voltage under the conditions of highly variable incoming voltage. The key element of an intelligent distribution system is the AC controller and, besides acceptable mass and size parameters, the device should possess high transformation efficiency and power factor, and low harmonic level in input current and output voltage [7–11]. In particular, for the AC voltage stabilization under the conditions of wide variation of input voltage, the AC voltage controllers are needed which are able to regulate higher and lower voltage in reference to nominal level. Efficient solution can be obtained by using a controllable pulse-width modulated (PWM) electronic supply-line transformer (ESLT) based on a resonance structure with switching capacitor [12,13]. It should be noted that ESLT are widely applied in local smart building systems, industrial equipment and high-power electrical sources. In the present study, the ESLT is designed where, besides PWM regulation of output voltage, the soft switching mode of semiconductor switches, decreasing dynamic power loss due to switching at zero current, is applied.

2. Electronic transformer

The schematic diagram of power circuit of ESLT is shown in Fig. 1. As compared with the earlier technical solution [12], the considered ESLT has less transistor switches and is equipped with overvoltage protection of the switches during switching of reactor L_1. In addition, the bulky output capacitor is absent and the power

* Corresponding author at: Institute of Semiconductor Physics, SB RAS, Novosibirsk 90, Russia.
E-mail address: atuchin@isp.nsc.ru (V.V. Atuchin).

http://dx.doi.org/10.1016/j.ijepes.2017.03.004
0142-0615/

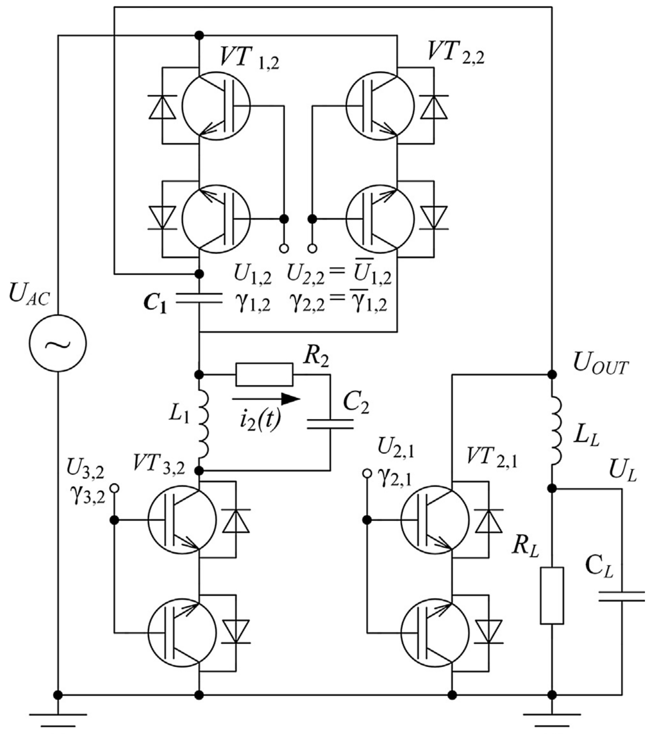

Fig. 1. Schematic diagram of controllable ESLT PwC.

capacitor C_1 capacitance is two times less that leads to great decrease of ESLT mass and size. The voltage at all transistor switches in closed state is not above the line source, as distinct from common AC regulators [14].

For different regulating ranges, the conversion coefficient (transformation factor) K_C of the ESLT structure is different. When K_c changes in the range of 0–1, the ESLT becomes step-down PWM AC regulator based on bidirectional transistor switches $VT_{1,2}$, $VT_{2,1}$ operating in inverse regime. Regulating is carried out by simultaneous changing frequency normalized with respect to the conversion period (transformation period) T_c and duration $\gamma_{1,2} = \overline{\gamma}_{2,1}$ of controlling pulses $U_{1,2} = \overline{U}_{2,1}$ by bidirectional transistor switches $VT_{1,2}$ and $VT_{2,1}$ in the range from zero to one. In this case, the bidirectional transistor switches $VT_{2,2}$, $VT_{3,2}$ are cut-off. The bidirectional transistor switch $VT_{2,1}$ is required for eliminating current interruptions via smoothing reactor L_L during closing of switch $VT_{1,2}$. When K_C changes in the range of 1–1.5, the ESLT works as a resonance step-up PWM AC regulator based on the step-up converter unit (SUCU) with switching capacitor C_1 [13]. It consists of the series oscillatory loop (L_1, C_1) and bidirectional transistor switches $VT_{1,2}$, $VT_{2,2}$, $VT_{3,2}$. The resonance frequency of the loop coincides with the ESLT conversion frequency f_C which is equal to the switching frequency of the transistor switches that are part of the ESLT. In the first range, the increase of EF is reached by decreasing dynamical power losses concerned with switching of bidirectional transistor switch $VT_{3,2}$ owing to switching at the time moments when the current through the switch is zero.

In the second range, the regulation of K_C is carried out by the inverse PWM regulation of bidirectional transistor switches $VT_{1,2}$ and $VT_{2,2}$. The normalized regulation pulse duration $U_{2,2}$ is being changed by the bidirectional transistor switch $VT_{2,2}\gamma_{2,2} = \overline{\gamma}_{1,2}$ in the range from 0 to 0.5 and coefficient $\gamma_{2,1}$ varied in the range from 0.5 to 1. For the step-up case, the bidirectional transistor switch $VT_{2,1}$ is cut-off. Controlling the bidirectional transistor switch $VT_{3,2}$ is carried out by the rectangular pulses $U_{3,2}$ of the constant duration $0.5 \cdot T_C$. The switching frequency f_C is the same for all ESLT power circuit transistor switches. Controlling ESLT transistor switches in different regulation ranges is conducted in accordance with the control matrices which elements describe control signals $U_{i,j}$ of corresponding transistor switches $VT_{i,j}$.

$K_C = (0 \div 1) \qquad K_C = (1 \div 1,5)$

$$\begin{vmatrix} & X(\sim) \\ \bar{X}(\sim) & 0 \\ & 0 \end{vmatrix} = \begin{vmatrix} & U_{1,2} \\ U_{2,1} & U_{2,2} \\ & U_{3,2} \end{vmatrix} = \begin{vmatrix} & \bar{X}(\sim) \\ 0 & X(\sim) \\ & X \end{vmatrix},$$

where $U_{3,2} = X$ is the control signal that is the periodic sequence of rectangular pulses of the period $T_c = \frac{1}{f_c}$ and duration $0.5 \cdot T_c$. $U_{2,2} = X(\sim)$ is the control signal that is the periodic (with the period $T_c = \frac{1}{fc}$) sequence of rectangular pulses with the duration controlled within the range from 0 to $0.5 \cdot T_c$. The signal $X(\sim)$ is delayed with respect to the signal X by $0.5 \cdot T_c$; $U_{1,2} = \bar{X}(\sim)$ is the inverted signal $X(\sim)$ and 0 is the control signal providing cut-off of the corresponding transistor switch. The time diagrams explaining ESLT operation for both regulation ranges of K_C are represented on Fig. 2.

3. Operation

The principle of operation is following. When the transistor switches $(VT_{1,2}, VT_{3,2})$ are on, the capacitor of the series (L_1, C_1) loop is being charged from the line source U_{AC} which instantaneous value is E_1. Simultaneously, the source U_{AC} charges the load inductance L_L through the "on" transistor switch $VT_{1,2}$. Then, the transistor switch $VT_{2,2}$ is closed leading to discharge via the load of the serially connected source $U_{AC} = E_1$, capacitor C_1 (charged up to the voltage E_1) and inductance L_L. As a result, the output voltage U_{OUT} changes within the range from E_1 to $2 \cdot E_1$, smoothed by filter (L_L, C_L) and has the maximum average value $U_{L(\max)} = 1.5 \cdot U_{AC(\max)}$. The ESLT output current has two equal components. The first is generated by the capacitor C_1 discharge and the second directly goes to the load from the line source U_{AC} during the reactor L_L discharge through the closed transistor switch $VT_{1,2}$. As a result, the current provided by the capacitor C_1 to the load, and hence its capacitance, are decreased by a factor of two. The capacitance C_1 is determined from the condition that the average value of its discharge current be equal to one half of the maximum load current amplitude, i.e.

$$I_{dC1}(AV) = \frac{1}{T_c} \cdot \int_0^{\frac{T_c}{2}} I_{dC1}(t) \cdot dt = 0.5 \cdot I_{L(\max)}.$$

This means that the voltage pulsation value on the capacitor ΔU_{C1} is determined by the expression

$$\Delta U_{C1} = \frac{1}{C_1} \cdot \int_0^{\frac{T_c}{2}} I_{dC1}(t) \cdot dt = \frac{I_{L(\max)}}{2 \cdot C_1 \cdot f_c}.$$

Because the maximum power at the ESLT load is determined by the product of maximal effective voltage and current, the relation is fulfilled:

$$P_{L(\max)} = U_{LEff(\max)} = 1.5 \cdot U_{ACff(\max)} \cdot I_{LEff(\max)}.$$

Then, we obtain

$$C_1 = \frac{I_{L(\max)}}{2 \cdot f_C \cdot \Delta U_{C1}} = \frac{I_{LEff(\max)}}{2 \cdot f . \delta_{C1} \cdot UACEff(\max)} = \frac{P_{L(\max)}}{3 \cdot f_C \cdot \delta_{C1} \cdot U^2_{ACEff(\max)}}$$

where $U_{ACEff(\max)}$ - is the maximum root-mean-square value of the line voltage U_{AC}; $I_{LEff(\max)}$ - is the maximum root-mean-square value of the load current; $\delta_{C1} = \frac{\Delta U_{C1}}{UACEff(\max) \cdot \sqrt{2}}$ - is the maximum allowed