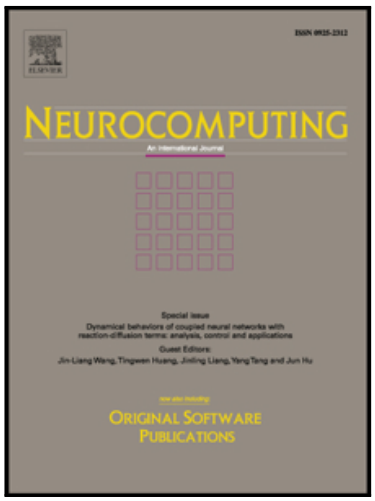

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Hardware Architecture for Large Parallel Array of Random Feature Extractors applied to Image Recognition

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Abstract

We demonstrate the use of a low-power and compact hardware implementation of Random Feature Extractor (RFE) core in image recognition applications. We show that weight distributions with zero mean are necessary for good performance in this application. We also show the performance in this application of a recently proposed weight reuse technique that virtually expands the number of random features available from RFE core. Further, we propose a method of reducing computation cost by pruning "incognizant" or redundant random feature neurons. For proof of concept, we validated our approach by using our RFE core as the first stage of Extreme Learning Machine (ELM)–a two layer neural network–and using 12800 hidden neurons were able to achieve upto 97.8% accuracy on MNIST database of handwritten digits. The RFE ASIC occupies 5 mm $\times$ 5 mm area in 0.35μm CMOS process. By using the proposed pruning method, an accuracy of 97% is obtained by using only 4749 effective hidden neurons and consuming 6.1 μJ/classify. Input pre-processing and ELM second stage requiring just addition operations can be implemented using digital adders with estimated power consumption of 24.9 nJ/classify. With a total energy consumption of only 6.12 μJ/classify, this low-power mixed signal ASIC can act as a co-processor in portable electronic gadgets with cameras.

Key words: Random Feature Extraction, neural network hardware, Extreme Learning Machine (ELM), sub-threshold VLSI, energy-efficient neural network

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