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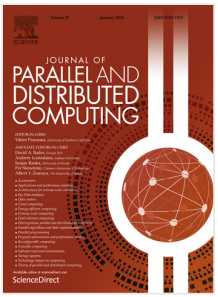

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Architecture Level Analysis for Process Variation in Synchronous and Asynchronous Networks-on-Chip

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ABSTRACT

Synchronous NoCs suffer from performance degradation due to clock skew. Clock skew is more pronounced with process variation (PV). Although asynchronous NoCs suffer from handshaking overhead, their immunity to PV is better than synchronous networks which would favor them in terms of throughput. Architecture-Level analysis aims to determine the ability of different NoC communication schemes to mitigate the impact of PV. The proposed analysis depends on redeveloped simulator which is unique PV-aware simulator for both synchronous and asynchronous NoCs.

Architecture-Level simulation shows that clock skew causes significant performance degradation in synchronous networks. Clock skew represents 27% and 32% of the delay variation for 45nm and 32nm technologies, respectively. Using real traffic, Architecture-Level analysis shows considerable throughput reduction for synchronous NoC under PV conditions. Throughput degradation of synchronous NoC increases rapidly with technology scaling down. 64-Cores synchronous NoC loses 30% of the nominal throughput for 45nm technology and 41% of throughput for 32nm with PV. On the other hand, 64-Cores asynchronous network throughput degradation is 12% and 13.6% for 45nm and 32nm technologies, respectively. For different NoC dimensions and using different workloads, throughput reduction for synchronous design is more than double the reduction of asynchronous design. Asynchronous scheme is preferable as technology scales.

KEYWORDS: NoC; Process variation; Throughput; Asynchronous router; Synchronous router; clock skew; Architecture Level Simulator.

1. INTRODUCTION

Network-on-Chip (NoC) is proposed to satisfy the rapid increase in communication demands of VLSI circuits. NoC allows the designers to embed complex processing elements (PE) into single chip [1]. Data transfer in NoC could be performed synchronously or asynchronously. Synchronous NoC uses global clock to synchronize the entire chip. On the other hand, asynchronous NoC relies on handshaking protocols [2]. Though, asynchronous network suffers from delay and area overheads [3], built-in flow control in bundled-data NoC is introduced to gain enhancement in terms of latency and area compared to synchronous counterparts [4].

Deviation of process parameters from their nominal values is known as process variation (PV). PV becomes more significant with fabrication technology scaling down. Higher network delay, more power consumption [5], performance degradation and frequency reduction [6] are direct impacts of PV. Fabricated gates vary in terms of influenced parameters such as threshold voltage and gate length which are the most sensitive parameters to PV [7]. The impact of interconnect delay is not negligible any more with the advance in manufacturing technology. Interconnect delay has a negative impact in propagation delay and network performance [8]. Under PV conditions, synchronizing processing elements becomes more challenging. PV causes clock skew and affects the maximum frequency that could be sustained among PEs [9]. Many researchers paid attention to avoid or decrease clock skew, and improve overall network performance and power profile [10,11]. 3×3 PV-influenced synchronous NoC is shown in Figure 1. Each