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Inverting voltage buffer based lossless grounded inductor simulators

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ABSTRACT

In this study, two new lossless grounded inductor simulators (GISs) made up of a single plus-type second-generation current conveyor, two inverting voltage buffers and a minimum number of passive components are proposed. There is no requirement of matching conditions and cancellation constraints among passive elements of the proposed GISs. Nevertheless, both of the proposed GISs have a floating capacitor which can be easily realized in nowadays integrated circuit fabrication. A second-order voltage-mode band-pass filter application is given for the proposed lossless GISs. A number of simulations based on SPICE program are given so as to verify the theory.

1. Introduction

Physical spiral inductors have been widely used for a number of years. Nevertheless, they are usually unwanted components in integrated circuits (ICs) because of the fact that they have magnetic properties, low quality factors, small and non-tunable inductor values, low self-resonance frequencies and the requirements of large silicon areas. Thus, simulated inductors [1–46] have been employed instead of physical spiral inductors in IC technology.

In the open literature, a number of floating inductor simulators [1–23,45,46] and grounded inductor simulators (GISs) [24–46] based on different active elements have been presented. However, previously presented GISs [24,27–33] employ two or three number of second-generation current conveyors (CCIIs). Some GISs are composed of inverting and non-inverting type CCIIs [24,27]. Some of the GISs consist of four or more passive elements [25,26,28,30,31,33,34]. Several GISs are made up of a complex internal structure [31,33,35,40,41,45]. Some of them require passive components matching conditions [25,26,30,31,33,35–38,45]. Several GISs [39,41,42] are lossy. Some GISs [43,44,46] use operational transconductance amplifier (OTA) in their internal structure; thus, their high frequency operation is limited [47]. Apart from these, Yuce and Minaei proposed a GIS employing three current-feedback operational amplifiers (CFOAs) and four passive components [34]. The GIS reported by Soliman uses a single plus-type CCII (CCII+) and five passive elements [25]. Also, it needs two critical passive element matching conditions and cancellation constraints. The main features of the presented grounded inductor simulators in [24–46] and the proposed ones are summarized in Table 1.

In this paper, we propose two new lossless GISs employing a single CCII+, two inverting voltage buffers (IVBs), two resistors and a capacitor. Both of the proposed GISs do not require any critical passive component matching conditions and cancellation constraints. The IVB can be easily constructed by using only two MOS transistors operated in the saturation region. A self-biasing MOS transistor based CCII+ with very low parasitic resistor at X terminal is selected to increase low frequency performance of the second proposed GIS. Hence, the second proposed GIS can be operated roughly between 200 Hz and 10 MHz. A voltage-mode (VM) band-pass (BP) filter given as an application of the proposed lossless GISs can be operated in a wide frequency range. Thanks to self-biasing technique on the CCII+, any biasing voltages and/or biasing currents except two DC symmetrical supply voltages are not used. Implementation of the lossless GISs is composed of twenty MOS transistors.

This work is organized as follows: After the introduction is given in Section 1, both of the proposed GISs are treated in Section 2. After parasitic resistor effects on the performance of both of the lossless GISs are investigated in Section 3, an application example such as second-order VM BP filter is given in Section 4. After a number of simulations are achieved in Section 5, this study is concluded in Section 6.

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Table 1
Comparison of the previously presented grounded inductance simulators [24–46] and the proposed ones.

References	# of active elements	# of floating/grounded passive elements	# of transistors	Area [a,b]	Matching condition	Operating frequency ranges	Biasing voltage/ current source	Electronic Tunability
[24]	1 CCII-, 1 CCII+	0/3	NA	NA	No	NA	NA	No
[25]	1 CCII+	3/2	NA	NA	Yes	NA	NA	No
[26]	1 CCII+	4/2	NA	NA	Yes	NA	NA	No
[27]	1 CCII-, 1 CCII+	0/3	AD844	NA	No	NA	No	No
[28]	3 CCII+	0/4	AD844	NA	No	NA	No	No
[29]	3 CCII+	0/3	AD844	NA	No	NA	No	No
[30] in Fig. 1	2 CCII+	1/3	AD844	NA	Yes	NA	No	No
[31] in Fig. 4	3 CCII+	1/3	30	191.1 μm^2	Yes	30 kHz to 200 MHz	Yes	No
[32] in Fig. 1	2 CCII+	0/3	NA	NA	No	NA	NA	No
[33] in Fig. 7	3 CCII+	1/3	30	219 μm^2	Yes	1 Hz to3 MHz	Yes	No
[34]	3 CFOA	1/3	AD844	NA	No	NA	No	No
[35] in Fig. 2b	1 DXCCII	2/1	48[c]	276.6 μm^2	Yes	NA	Yes	No
[36] in Fig. 3b	1 DXCCII	1/2	29[c]	155.8 μm^2	Yes	30 kHz to 30 MHz	Yes	No
[37] in Fig. 2a	1 DXCCII	2/1	28	142.2 μm^2	Yes	100 Hz to 10 MHz	Yes	No
[38]	1 DCCII	1/2	27 (BJT)	NA	Yes	NA	Yes	No
[39]	1 CDBA	2/1	AD844	NA	No	NA	No	No
[40]	1 ZC-CCCITA	0/1	31	563 μm^2	No	14 kHz to 21 MHz	Yes	Yes
[41]	1 OTRA	2/0	14	2075 μm^2	No	NA	Yes	No
[42]	1 OTRA	3/0	20	NA	No	NA	Yes	No
[43] in Fig. 2a	1 VDCC	0/2	22	132.3 μm^2	No	30 kHz to 20 MHz	Yes	Yes
[44]	1 VDBA	2/0	2 OPA860	NA	No	10 kHz to 10 MHz	No	Yes
[45] in Fig. 5	1 MDO-DDCC	1/2	18	267.3 μm^2	Yes	5 kHz to 700 kHz	Yes	No
[46]	1 VD-DIBA	1/1	22	144.5 μm^2	No	NA	Yes	Yes
The first GIS	1 CCII+, 2 IVF	2/1	20	155.2 μm^2	No	200 kHz to 20 MHz	No	No
The second GIS	1 CCII+, 2 IVF	2/1	20	155.2 μm^2	No	200 Hz to 10 MHz	No	No

NA: not available.
[a] Sum of products of the lengths and widths of each transistor in the CMOS structures.
[b] Ideal current source assumed.
[c] Z terminals must be copied according to the CMOS realization.

2. The proposed grounded inductor simulators

Electrical symbols of the CCII+ and IVB are respectively shown in Figs. 1and 2. The CCII+ and IVB are respectively described by the following matrix equations:

$$\begin{bmatrix} V_x \\ I_y \\ I_{z+} \end{bmatrix} = \begin{bmatrix} \beta & R_X & 0 \\ 0 & 0 & 0 \\ 0 & \alpha & 1/R_{Z+} \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_{z+} \end{bmatrix} \tag{1a}$$

$$\begin{bmatrix} V_x \\ I_y \end{bmatrix} = \begin{bmatrix} -\gamma & R_B \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \end{bmatrix} \tag{1b}$$

where β and γ are non-ideal voltage gains of the CCII+ and IVB, respectively. Further, α is a current gain of the CCII+. Non-ideal voltage gains can be defined as $\beta = 1 + \varepsilon_\beta$ and $\gamma = 1 + \varepsilon_\gamma$ in which voltage tracking errors are identified as $|\varepsilon_\beta| \ll 1$ and $|\varepsilon_\gamma| \ll 1$. In a similar way, the non-ideal current gain can be defined as $\alpha = 1 + \varepsilon_\alpha$ where current tracking error is defined as $|\varepsilon_\alpha| \ll 1$. β, α and γ are ideally equal to unity and their signs are positive. R_X and R_B in series are respectively X terminal parasitic resistors of the CCII+ and IVB, which are ideally equal to zero. Also, R_{Z+} in parallel is the Z+ terminal parasitic resistor, which is ideally equal to infinity.

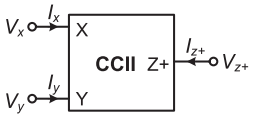

Fig. 1. Electrical symbol of the CCII+.

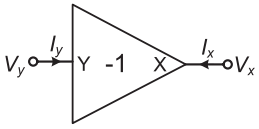

Fig. 2. Electrical symbol of the IVF.

The first proposed lossless GIS consists of two IVBs and one CCII + as active components and two resistors and a single capacitor as passive elements. Further, the electrical equivalent circuit of the proposed lossless GIS in Fig. 3 is given in Fig. 4 where $L_{eq} = CR_1R_2$. The input impedance of the first proposed lossless GIS in Fig. 3 is ideally obtained by using the port relation of active elements as in the following:

$$Z_{in} = \frac{V_{in}}{I_{in}} = sCR_1R_2 \tag{2}$$

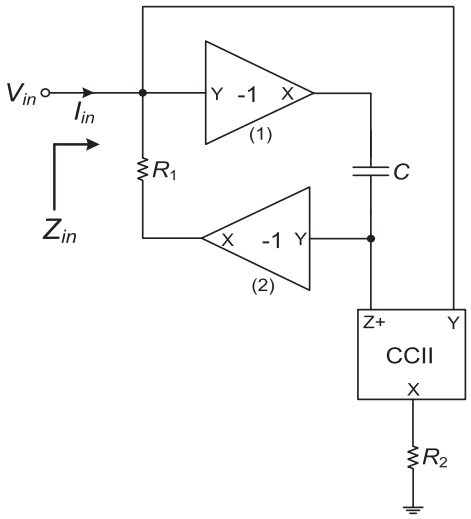

Fig. 3. The first proposed lossless grounded inductor simulator.