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Low power dynamic circuit for power efficient bit lines

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ABSTRACT

In this paper, a low power dynamic circuit is presented to reduce the power consumption of bit lines in multi-port memories. Using the proposed circuit, the voltage swing of the pull-down network is lowered to reduce the power consumption of wide fan-in gates employed in memory's bit lines. Wide fan-in OR gates are designed and simulated using the proposed dynamic circuit in 90 nm CMOS technology. Simulation results show at least 40% reduction of power consumption and 1.2X noise immunity improvement compared to the conventional dynamic circuits at the same delay. Exploiting the proposed dynamic circuit, wide fan-in multiplexers are also designed. The multiplexers are simulated using a 90 nm CMOS model in all process corners. The results show 41% power reduction and 27% speed improvement for the proposed 128-input multiplexer in comparison with the conventional multiplexer at the same noise immunity.

1. Introduction

Dynamic circuits are typically employed in read-out paths of register files and multi-port memories due to their advantages over the static ones. Main building blocks of read paths include local and global bit lines. Bit lines consume significant portion of the total dynamic power in the read-out path. As stated in [1], bit lines consume nearly 70% of the dynamic power in the register files. The power consumption of bit lines becomes the dominant factor in energy breakdown of memories as their size and number of read port are increased. Since bit lines are implemented using wide fan-in dynamic gates, power consumption of read-out paths can be reduced by using low power dynamic circuits.

A conventional dynamic circuit is shown in Fig. 1. It needs a keeper transistor to maintain the level of the dynamic node against charge sharing, leakage current and noise sources. However, delay and power consumption of the dynamic circuit increases due to the contention between the keeper transistor and the pull-down network. As the technology scaled down, the leakage current exponentially increases because of low threshold voltage and accounts for a dramatic portion of the overall power consumption [2]. This becomes even up to 50% in the 90 nm technology [3]. Increasing the leakage current and crosstalk noise degrades the noise immunity, especially for wide fan-in gates due to the large number of leaky NMOS transistors connected to the dynamic node [4].

Although Keeper upsizing is a traditional way to maintain an acceptable noise margin level in deep sub-micron technologies, it increases current contention, yielding higher power consumption and delay. Therefore, there is a trade-off between noise immunity and delay. Since the keeper size affects on robustness and performance, the keeper ratio K is defined as:

$$K = \frac{\mu_p \left(\frac{W}{L}\right)_{Keeper-transistor}}{\mu_n \left(\frac{W}{L}\right)_{Pull-Down-network}} \quad (1)$$

where μ_n and μ_p are the electron and hole mobilities, respectively. Moreover, $\left(\frac{W}{L}\right)_{Keeper-transistor}$ and $\left(\frac{W}{L}\right)_{Pull-Down-network}$ are the aspect ratio of the keeper transistor and that of transistors in the pull-down network.

Several circuit techniques are reported in the literature to address the above-mentioned issues. While these techniques try to improve some design parameters, they degrade other parameters. The circuit techniques can be classified in two categories.

Designs in the first group change the keeper scheme [5–7] and the circuit techniques in the second group reconstruct the evaluation network [8–10].

As shown in Fig. 2(a), introducing a clock delay in the high speed domino (HSD) [5] can reduce the current drawn through the PMOS keeper and the NMOS pull-down network at the beginning of the evaluation phase. Therefore, HSD has a different keeper control scheme. In this circuit, when the clock goes to high state, the NMOS transistor M_{n1} is still off and the PMOS transistor M_{P2}

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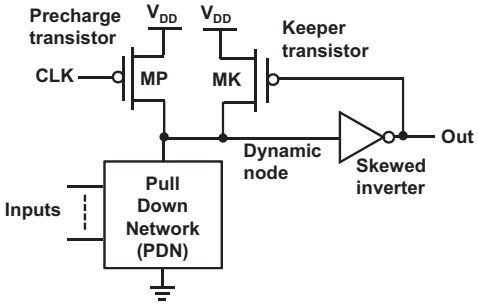

Fig. 1. Conventional dynamic circuit.

is still on. Thus, M_{P2} turns off the keeper transistor M_K. After the time delay of inverters, M_{P2} is turned off. If the dynamic node remains high during the evaluation phase, the NMOS transistor M_{n1} is turned on and caused the keeper transistor to go on.

However, the HSD suffers from the following drawbacks. Since the dynamic node at the beginning of the evaluation phase is afloat, any noise at the inputs could cause the evaluation node to be discharged in the absence of the keeper transistor. In additions, gate of M_K can be at V_{DD} -V_{tMn1} (V_{tMn1} is the threshold voltage of M_{n1}) and results in a DC current through the PMOS keeper transistor and the NMOS network.

As shown in Fig. 2(b), in the conditional keeper domino (CKD) [6] the strong keeper transistor was added to increase the noise immunity of the domino gate. This circuit employs two keeper transistors: a weak keeper to hold the state of the dynamic node during the transition of the NMOS logic and a strong keeper to be conditionally activated based on the state of the dynamic node after a certain delay during the rest of the evaluation phase. In this way the contention is reduced during the evaluation period, yielding higher speed and lower short circuit power dissipation. These all achieved at the expense of power overhead due to the inverter chain and NAND gate used for generating certain delay time.

A leakage current replica (LCR) keeper proposed by Lih et al. [7] to track the process, voltage and temperature (PVT) variations is shown in Fig. 2(c). This technique controls the strength of the keeper according to the process corners by using an analog current mirror to replicate the leakage current of the pull-down network. Although, this technique has lower standard deviation of delay time with process variations and employs only one extra transistor per gate plus a portion of a shared current mirror, it suffers from low robustness and high power dissipation, especially for wide fan-in gates.

Modified charging-scheme-based domino (MCSD) is another domino circuit proposed to reduce power consumption in wide fan-in gates [8]. As shown in Fig. 2(d), the parasitic capacitance on the dynamic node is reduced by partitioning the wide fan-in gates. In other words, this circuit technique divides the wide fan-in gates into 8-leg partitions by utilizing an enhanced diode. Therefore, the MCSD technique decreases delay of the wide fan-in gates at the cost of area overhead.

Current-comparison-based domino (CCD) was also proposed to decrease the contention current and power consumption [9]. As shown in Fig. 2(e), this technique employs a footer transistor in the diode-configuration to reduce leakage current and thus enhance the robustness of the circuit against sub-threshold leakage and input noise in deep submicron ranges. In this circuit, a mirrored current of the pull-up network is compared with a reference current to track process, voltage and temperature variations.

As shown in Fig. 2(f), voltage-comparison-based domino (VCD) circuit utilizes a footer transistor in diode configuration to decrease leakage current of transistors caused by the body effect. Also, a sense amplifier is utilized to determine the output state with regard to the voltages across the pull-down network [10].

This paper presents a modification on the conventional dynamic circuit in which evaluation circuit is changed to reduce the power consumption by lowering the voltage swing across the pull-down network. Moreover, using the proposed technique the noise immunity increases. In order to demonstrate the superiority of the proposed circuit over the existing circuits, wide gates with several fan-ins are designed and simulated.

The rest of this paper is organized as follows. The proposed dynamic circuit is presented in Section 2. In Section 3, simulation results and comparisons are explained. Implementation and

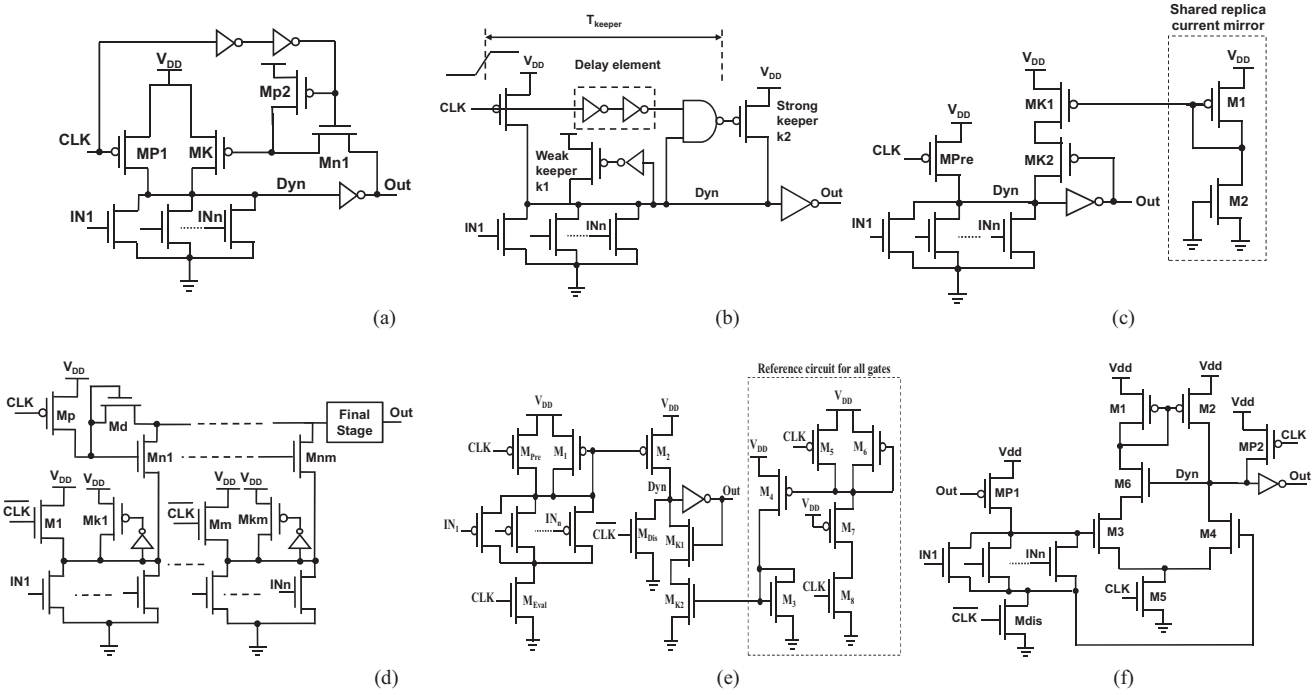

Fig. 2. Dynamic circuit techniques: (a) HSD [5], (b) CKD [6], (c) LCR [7], (d) MCSD [8], (e) CCD [9], (f) VCD [10].