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Design of ultra low power current mode logic gates using magnetic cells

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ABSTRACT

Non-volatile logic is a viable solution to overcome the leakage power issue which has become a major obstacle to CMOS technology scaling. Magnetic tunnel junction (MTJ)-based logic is a promising approach because of the non-volatility, less occupied area, almost zero static power consumption, programmability. This paper presents current mode logic gates using MTJ elements without any intermediate electronic circuitry. This efficient solution reduces the performance overheads of the spintronic logic circuits while simplifying fabrication. Hspice based simulations have been carried out to verify the performance of different logic gates. The simulation results reveal that the SBEG based gates provide less area, power consumption, and energy while also offering less design complexity as compared to mLogic (previously proposed magnetic logic) and CMOS gates.

1. Introduction

The continuous down scaling in CMOS integrated circuits has enabled the integration of a large number of transistors in a unit of area. This very high level of integration makes it possible for designers to implement very powerful computation platforms such as Chip Multi-Processors (CMPs). However, there are serious challenges such as power consumption and temperature that has limited the design of such powerful systems. Although technology scaling results in smaller parasitic capacitances and decreased power consumption per transistor, due to the high integration it will lead to the overall power consumption to be increased. Higher power consumption rises on-chip temperature which in turn poses serious challenges to the chip reliability and hardware system failures [1]. Operating voltage of circuit can be reduced to decrease dynamic/switching power consumption. However, reducing supply voltage results in reduced current driver of transistors which in turn, ends in circuit speed drop. Threshold voltage of transistors is also reduced to compensate the speed drop. However, reducing the threshold voltage leads to an exponential increase in transistors leakage current. Leakage power consumption caused by leakage currents has become a very important issue as it has the same contribution and even more as dynamic/switching power in total circuit power consumption in Nano-scale technologies [1–8]. Briefly, power consumption, required area, and performance issues are the main concerns that VLSI circuit designers will face. To provide an attractive trade-off between the mentioned design issues i.e. low power consumption, low occupied area, and high performance that are mostly conflicting, an emerging provision should be devised. Recently, designers are focused on design and implementation of circuits using Spintronic devices due to their great features such as: very low static power consumption, non-volatility, and low required area being more discussed in [9].

Spintronic devices are based on both the charge and the up and down spins of the electrons, rather than only on the charge of the electrons in traditional electronic devices. They define digital state as the orientation of magnetization in a ferromagnetic material with uniaxial anisotropy, which allows only two stable states (e.g. “up” and “down”). Because this information is stored as a magnetization direction, and not inherently dependent on an electrical power supply, it is non-volatile by its nature.

Magnetic tunnel junction (MTJ), shown in Fig. 1, is one of the spintronic devices, called mCell [10,11]. The mCell is a four-terminal element that has electrically isolated read path (R, R*) and write path (W−, W+). The principle of operation is based on a magnetic domain wall in the write path which is driven back and forth by an electric current. When the write path is magnetically coupled to the free layer of a magnetic tunnel junction, the resistance state of the read path changes as determined by the element’s tunneling magnetoresistance. We consider an mCell as a “black box” device with four terminals. Two terminals constitute a write-path, wherein the direction of input current flows to program the digital state of the device. The other two terminals include a read-path that is electrically isolated from the write-path. The state of the device is read out as a high or low resistance through the read-path terminals. By sending a small current pulse

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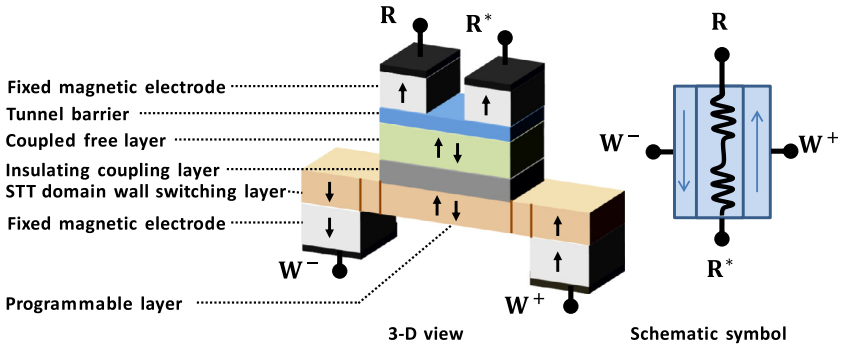

Fig. 1. mCell cross section, 3-D view, and schematic symbol. The read path of the mCell is through the (R, R*) terminals and the write path is through the (W−, W+) terminals [10].

from W− to W+ or W+ to W−, the mCell read path resistance between R and R* is changed to be high (RH) or low (RL), respectively. These two resulting resistance states are non-volatile, so that shutting off power has no effect on the direction of any layer's magnetization.

Non-volatile spin-torque switches can also be used in designing configurable logic blocks [12–46]. Such circuits can possibly provide enhanced scalability and energy-efficiency resulting from reduced-leakage of the spin-based memory elements. Exploiting these benefits of spin-torque devices, magnetic memories [12–16], magnetic logic circuits like full adders [17–41] non-volatile flip-flops [42–46], and hybrid FPGAs [47,48] have been proposed in literature. Consequently, circuits based on magnetologic elements which have many potential advantages, such as non-volatility, low power consumption, increased speed, and flexibility can be powerful competitors against transistor-based circuits. Despite the mentioned benefits, as opposed to pure transistor based circuits, there is no comprehensive standard and synthesis tool to produce gates and functions with magnetologic elements. Until recently, researchers have focused on design of specific circuits using magnetic cells and different magnetic logic circuits such as adders which have been designed and implemented. However, a design methodology for derivation of magnetic circuits from logic descriptions of different functions is a serious need [17–41]. In this work, a novel structure for all types of basic logic gates in pure magnetic logic circuits is proposed. The rest of this paper is organized as follows: Section 2 highlights previous researches in this research context. Section 3 presents the proposed structure and describes its details. Section 4 describes all types of basic logic gates implementation using the proposed structure. In Section 5 we compare our gates with mLogic (previously proposed magnetic logic) and CMOS gates. Section 6 states our final conclusions and perspectives.

2. Related work

With CMOS technology scaling to 90 nm and below, increasing chip density (# of transistors/unit of area) and cell leakage have caused the static power of circuits to dominate the overall power consumption of the latest microprocessors. Many circuit design and architectural solutions, such as VDD scaling [49], power-gating [50], and body-biasing [51], have been proposed to reduce the static power of circuits. However, these techniques are becoming less effective as technology scaling has caused the transistor's leakage current to increase exponentially. The International Technology Roadmap for Semiconductors (ITRS) has reported that the static power will be the major part of total power consumption of systems in future [52]. To solve the power dissipation problem, researchers have focused recently on circuits based on MTJ due to MTJ's significant features especially its zero static power. We have divided these circuits into two significant categories: (a) Magnetic random-access memory (MRAM). (b) magnetic Logic circuits. In the following we will introduce the previous works in the mentioned categories.

MTJ-based MRAMs store data bits using magnetic charges instead of the electrical charges used by DRAM (dynamic random access memory) [12]. As reported by ITRS [52], MRAM is one of the most promising candidates to replace the traditional CMOS-based memories. In particular, the non-volatility of MRAM is a major advantage, which minimizes static power consumption. Among MRAM technologies, Spin-transfer torque MRAM (STT-MRAM) and Spin-Orbit Torque MRAM (SOT-MRAM) have gained a lot of attentions. STT-MRAM is non-volatile, scalable memory that has a low read access time [12,13]. In addition, due to the high resistance of the MTJ storage elements, STT-MRAM is compatible with the CMOS process. In particular, SOT-MRAM is gaining interest as it comes along with all the benefits of its predecessor STT-MRAM, but it is supposed to eliminate some of its shortcomings, especially, the split of read and write paths in SOT-MRAM that provides faster access times and lower energy consumption as compared to STT-MRAM [14,15].

Magnetic Logic circuits can be divided into two sub-categories: MOS/MTJ magnetic logic circuits [17–24], which are mainly consist of four parts: (1) a sense amplifier to evaluate the logic result on the outputs; (2) a volatile MOS logic block; (3) a non-volatile MTJ logic block; and (4) a writing logic block to write the MTJ cells. This type of logic circuits have good compatibility with conventional computing architectures and have easy integration with the existing MOS technology process. The opposite of MOS/MTJ magnetic logic circuits are pure magnetic logic circuits which are entirely based on MTJ cells. MTJ cells are configured into current steering based circuits. This type of logic circuits can operate on very low, noisy supply voltages [25,32].

MOS/MTJ magnetic logic circuits employ transistors and MTJs for design of different circuits. This mandates the designer to use voltage-to-current (V/I) convertor as transistors are voltage-controlled switches while MTJs are current-controlled switch elements. In addition, as the outputs should be in voltage mode, it is needed to employ Sense Amplifiers (SA).

Employing SA and V/I convertors have the following disadvantages. First, in these circuits, as transistors are used, they suffer from process variation issue which seriously challenges the circuit reliability. Second, SA and V/I make a circuit hard to accomplish any pre-fabrication predictions, testing and debugging, especially for complex circuits (like microprocessors). Third, they increase area overhead and fourth, having SAs and Convertors increases the complexity of CAD tools for 3D ICs as they should take into