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Pseudo differential multi-cell upset immune robust SRAM cell for ultra-low power applications☆

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ABSTRACT

This paper presents a pseudo differential 12 transistor (PD12T) ultra-low leakage, fully half-select-free robust SRAM cell with good static and dynamic read/write performance. The proposed cell offers best Read/Hold SNM, Write Margin (WM) and least leakage power among all the cells considered in this work while causing an area overhead of 2.5× of that of 6T cell. Simulation results at V_{DD} = 0.5 V show that PD12T cell offers 4.24× higher RSNM, 1.62× higher WM, 1.9× smaller leakage power (at 50 °C) as compared to 6T SRAM. The proposed cell offers $V_{DD,min}$ = 140 mV which is 260 mV smaller than that for 6T cell. When operated at $V_{DD,min}$, the proposed cell consumes 13.6× smaller mean leakage power. The Ion/Ioff ratio of the proposed cell is more than 10× as compared to 6T cell and it holds potential to compensate for the area overhead by having more number of cells connected to the same bitline. The proposed cell is also suitable for all-TFET implementation as it requires only unidirectional current flow through transistors. Monte Carlo simulations using HSPICE with 16 nm PTM were performed by incorporating local and global variations and it is observed that the proposed cell offers high robustness against PVT variations. The proposed cell has highest critical charge among all other considered cells, which means that it is least vulnerable to soft-errors. The proposed PD12T also offers the best Electrical Quality Metric (EQM) among the cells considered in this work. The MC simulations for HSNM of row and column half-selected cells show that the mean value of SNM is approximately 30% of V_{DD}. Therefore, the proposed cell can be used for bit-interleaving architecture to achieve multi-cell upset immunity and could be a good choice for applications that demands high stability, moderate speed and ultra-low power.

1. Introduction

SRAM is an important building block in computing systems that consumes significant fraction of power. Major share of the static power consumption is attributed to the SRAM as they occupy more than 50% of the chip area [1,2]. In the present scenario, low power applications like wireless sensor nodes, implantable biomedical devices and other battery operated portable devices require ultra-low leakage power SRAM cell. One of the popular solutions to reduce leakage and active power is to operate SRAM in near/sub-threshold region. However, increased variation in modern scaled technology puts a major challenge in the SRAM design at lower operating voltages [3]. σV_{th} of devices has increased significantly with continuous scaling of the device geometry [4]. Consequently, Read/Write failure probability has significantly increased due to the difficulty in maintaining the Cell-ratio and Pull-up-ratio in conventional 6T SRAM cell. Many circuit techniques have been proposed to decouple the read/write path [5–12] to address these issues in conventional 6T SRAM cell. Decoupling read/write path improves the cell stability and also improves $V_{DD,min}$ that can be exploited to reduce the static leakage power significantly [11,12].

The soft-error is one of the key issues in SRAMs and is more problematic in subthreshold regime due to the reduction of critical charge, Q_C [13]. As technology advances, the decreased storage node area mitigates the chances of single-event upsets (SEUs), which is soft-error per memory bit [14]. However, with the technology scaling, the effective distance between transistors decreases, which increases the chances of simultaneous errors in more than one memory cell induced by a single ion strike resulting in multiple-cell upsets (MCUs). Thus, MCUs in SRAMs due to ion strikes have increased significantly, in spite of decrease in SEU per bit [14,15]. Fig. 1 shows the increasing trend of ratio of MCUs to SEUs as a function of technology node [15]. The checkerboard signifies the bit pattern of consecutive 1's and 0's. This poses a serious threat to the functionality of SRAMs since MCUs cannot be recovered by conventional Error Correction Schemes as they can detect and correct only single bit errors. Bit-interleaving technique is used to deal with these errors efficiently. However, use of bit-

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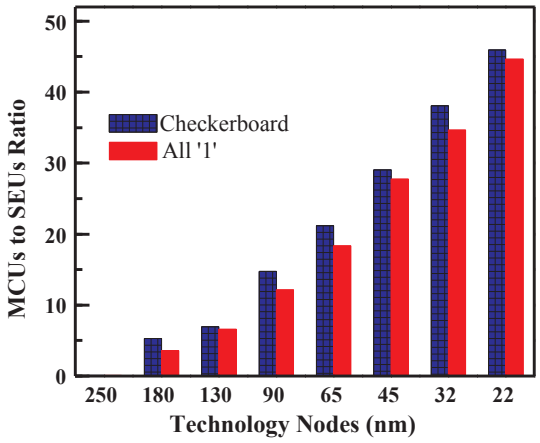

Fig. 1. Ratio of MCUs to SEUs for SRAM cells as a function of technology nodes [15].

interleaving architecture results into Half Select (HS) issue in most of the SRAM cells [16]. While the existing works address the read/write stability of the selected cell, stability issues in column/row HS cells has not been fully addressed. In most of the recent work, HS issue is handled by techniques such as write-back [5,17,18], array architecture approach [19–21], local write wordline [22], and hard-coding [23,24] etc. that incur power and performance penalties. Recently 12T bit-interleaving cell, BI12T [13] and a power gated 9T cell, PG9T [25] have been proposed to solve the HS issue without using these techniques. However, BI12T suffers with very precise WL pulse requirement to mitigate the degradation of floating data at storing nodes Q or QB in column HS cells during write operation. Similarly, PG9T cell also suffers from floating storage node in row HS cells. It also suffers with

poor write-ability and longer write delay due to stacked transistor and conflicting charging and discharging of internal node between the access transistors while writing '0'. Therefore, in this work, we present a 12-transistor pseudo differential SRAM cell (PD12T) that is fully half-select free thus doing away with the write-back or any other assist techniques and supports a bit-interleaving architecture to improve MCUs immunity. The proposed cell also improves write-ability without using additional peripheral write-assist circuits. Furthermore, the proposed cell requires only unidirectional current flow through transistors; and hence. it is also suitable for all-TFET implementation.

The rest of this paper is organized as follows. In Section 2, cell structure and functioning of PD12T is discussed. Section 3 presents the simulation setup, results and comparison of the SRAM cells considered in this work and Section 4 concludes this paper.

2. Pseudo differential 12T (PD12T) SRAM cell

Fig. 2 shows the schematic diagram of the proposed PD12T SRAM cell. The PD12T cell consists of a cell core (cross coupled inverter along with power cutoff switches MPL1, MPL2, MPR1 and MPR2), read access path consisting of two transistors (MR1 and MR2) and write-access path consisting of three transistors (MAL, MAR and MD). The transistor MD, which is shared in a row, provides discharging path for storage nodes during the write operation. Table 1 illustrates the control signals in different modes of operation of the PD12T SRAM cell.

2.1. Read operation

During read operation, RWL is kept at '1' whereas all other control signals are grounded. This provides discharging path for precharged-RBL through transistors MR1 and MR2 depending on the data stored at QB. The column-based RWLB signal is utilized to eliminate bitline leakage in the read path of the unselected columns, which reduces the overall energy consumption. The disabled WLA, WLB and WWL signals

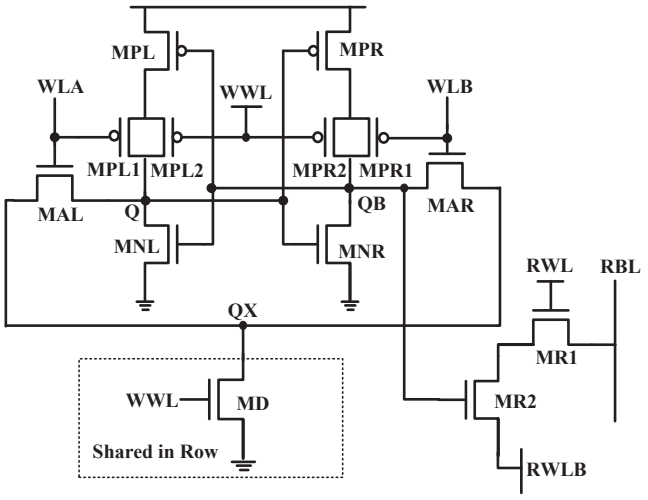

Fig. 2. Proposed SRAM cell.

Table 1
Operation table.

Control signal	Operation			
	Hold	Read	Write '0'	Write '1'
WLA	0	0	1	0
WLB	0	0	0	1
WWL	0	0	1	1
RBL	1	Pre	0	0
RWL	0	1	0	0
RWLB	1	0	1	1

makes data storage nodes (Q and QB) completely isolated from any disturbing path during the read access. Therefore, the read static noise margin (RSNM) of the PD12T cell is same as its hold SNM like that in conventional 8T cell. However, conventional 8T is not HS free.

2.2. Pseudo-differential write operation

Single-ended write [9,23,26,27] reduces the leakage and switching power while incurs penalty in terms of increased write-access time and degraded write margin (WM). In fact, it requires some assist techniques such as dual V_{th} [5], asymmetric write assist [23,26], power-cutoff [27] for good write-ability. On the other side, differential write cells such as 6T, CONV8T consume significant Bitline switching power, but improve write performance. In the proposed cell, the write-ability is as good as of differential write cells, whereas active power is as low as that of single-bitline cells. The write operation in PD12T cell is, in fact, single-ended, but it involves only writing of '0' similar to differential write. The Write '0' or Write '1' operation are accomplished by writing '0' at node Q or QB respectively. Fig. 3 illustrates the write '0' operation in the selected cell along with row and column half-selected cells. The WWL and WLA are kept at '1' whereas WLB is grounded. The left inverter of selected cell is completely cut-off from power supply and node Q is easily discharged through transistors MAL and MD. Similarly for write '1', the WWL and WLB are'1' whereas WLA is kept at '0'. The supply is now cut-off for right inverter and node QB is discharged easily through MAR and MD. Consequently '1' is written at node Q. Since, for either write operation, only one write path is active, therefore, we call it pseudo differential write operation.

3. Simulation results and discussion

This section presents simulation results and discussions based on the simulation setup described below: