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Response of ring oscillator to periodic interference on the power supply

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ABSTRACT

Periodic noise is one of the most common interference sources in the power distribution network of integrated circuits. It is well known that this noise can deleteriously affect timing margins and limit the circuit performance. This paper presents a theory on the response of ring oscillators in presence of periodic interference on the power supply. The theory links the cycle time of ring oscillators to the probability density function of the interference. Various waveforms of interference are studied, such as sinusoidal, triangular, and square. In addition, symmetrical and asymmetrical interference waveforms are also considered. Both transistor level HSPICE simulations and real measurements are performed to validate the theory. The obtained results are suitable with the model over a wide range of interference frequency. The valid range of the model, multi-tone interference, and methods to reduce the sensitivity of ring oscillators are also discussed.

1. Introduction

With the trend of increasing operating frequencies and decreasing supply voltage, avoiding electromagnetic interference (EMI) in circuits and electronic systems has become a serious problem [1–5]. Moreover, existing circuits are also more sensitive to interference. Therefore, the behavior of on-chip digital circuits under EMI on the power supply stands as an important research field. EMI can be either periodic or random, the former being more common and stronger, given the existence of external and on-chip sources that generate periodic noise on the power distribution network through conduction or radiation. Research shows that the propagation delay of a circuit varies under interferences, which affects deleteriously timing margins and limits the circuit performance [6]. A ring oscillator (RO), built with inverters, is a basic block for several electronic systems and a commonly used device under test (DUT) to study the propagation delay problem [7,8].

Few theories have been developed to analyze the behavior of RO subjected to periodic supply noise. Refs. [9,10] point out that sidebands appear in the spectrum of the RO output, produced by small-amplitude radio frequency noise on the power supply. In addition, the magnitude of sidebands is disproportional to the amplitude of injected noise. In [11], the authors note that the cycle jitter of the RO is independent from interference frequency due to sinusoidal supply voltage disturbances based on quasi-static approximations. The studies in [12,13] demonstrate that the gate-delay variation caused by triangular supply noise is more relevant to the average value of supply voltage drop than the noise peak. Ref. [14] shows that under sinusoidal modulation, the variation in the propagation velocity of the clock distribution is proportional to the modulation frequency. Finally, based on the response of RO to DC voltage, an RO is used to capture supply noise waveforms in [15,16].

These previous works have studied the instantaneous response of RO and focused on the random phase variation under small-amplitude periodic disturbances on the power supply. On the other hand, this paper focuses on the operation frequency of RO in the presence of high amplitude periodic interference (PI) on the power supply.

Different PIs show both positive and negative disturbances, causing the gate delay of RO to decrease in one half cycle and increase in the other half cycle. When the impact of positive disturbances balances that of negative disturbances, there may be a net frequency shift of RO. The purpose of this paper is to study the net influence of interference on the cycle time of ROs.

The rest of this paper is organized as follows. In Section 2, we examine the operational cycle time of RO using analytical deduction. The model shows that the net frequency shift of the RO can be calculated based on the static response of the gate delay and the probability density function of PI. In Section 3, we perform a series of simulations on ROs transistor-level models to verify the theoretical analysis. Measurement results are compared with the predicted values to validate the model in Section 4. The discussion about the valid range of the proposed model is given in Section 5. This section also shows the model application to multi-tone interference and a method used to reduce RO sensitivity. The final section provides the conclusion of this paper.

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2. Theoretical models

The basic RO is comprised of an odd number N_{RO} of inverters connected in a feedback loop. The signal passes through the chain of N_{RO} inverters twice to reach the initial state within a period; hence, a period corresponds to 2 N_{RO} switches of inverter output. In the absence of interference, the supply voltage V_{DD} of the oscillator is constant V_0. Each inverter is assumed to contribute an equal gate delay τ_0 to the period of the oscillator. The period of RO, T_{RO} can be calculated by (1). The N_s in (1) is the number of the switched inverters per time unit.

$$T_{RO} = \sum_{i=1}^{2N_{RO}} \tau_i(V_{DD}) = 2N_{RO}\tau_0 = \frac{2N_{RO}}{N_s} \tag{1}$$

The gate delay has a direct relationship with the supply voltage, called static response of inverter delay. Consequently, any variation in V_{DD} alters the inverters propagation delay. Under constant supply voltage, the steady-state output frequency of RO can be computed by (1). However, if fluctuations in V_{DD} are present, a more precise method to find this frequency is necessary.Consider the supply voltage fluctuates periodically in the presence of PI, as shown in (2). V_0 represents the nominal supply voltage, A_{PI} denotes the amplitude of PI, and f_{PI} is the PI frequency. Suppose that the interference cycle time T_{PI} is much larger than τ_0, such that a certain number of inverters switch during T_{PI}. During the gate switch, V_{DD} is approximately constant. From the above assumptions, the average value of the inverter switches under the interference per time unit $\overline{N_s}$, can be written as (3). The RO mean frequency, $\overline{f_{RO,PI}}$, is given by (4). With variable substitution, (4) can be converted into (6). The ρ parameter in (6) is the probability density function of V_{DD}.

$$V_{DD} = V_0 + A_{PI}(2\pi f_{PI} t) \tag{2}$$

$$\overline{N_s} = \frac{1}{1}\int_0^1 \frac{1}{\tau(V_{DD})} \tag{3}$$

$$\overline{f_{RO,PI}} = \frac{\overline{N_s}}{2N_{RO}} = \frac{\frac{1}{1}\int_0^1 \frac{dt}{\tau(V_{DD})}}{2N_{RO}} = \frac{\frac{1}{T_{PI}}\int_{t_0}^{t_0+T_{PI}} \frac{dt}{\tau(V_{DD})}}{2N_{RO}} = \frac{\int_0^{T_{PI}} \frac{1}{\tau(V_{DD})}\frac{dt}{T_{PI}}}{2N_{RO}} \tag{4}$$

$$\rho = \frac{dt}{T_{PI}}\Big|_{V_{DD}=V} \tag{5}$$

$$\overline{f_{RO,PI}} = \frac{\int_{V_1}^{V_2} \frac{1}{\tau(V_{DD})}\rho(V_{DD})dV_{DD}}{2N_{RO}} = \int_{V_1}^{V_2} \frac{1}{2N_{RO}\tau(V_{DD})}\rho(V_{DD})dV_{DD} = \int_0^1 \frac{1}{2N_{RO}\tau(V_{DD}(\rho))}d\rho \tag{6}$$

The symbol Δf_{RO_PI} represents the frequency shift owing to PI, thereby the normalized frequency shift (*NFS*) of RO is defined by (7), which is referred to as the response of RO to PI on the power supply. Combining (1), (6) and (7), we obtain the NFS of RO in (8). From both (6) and (8), we can note that the number of inverters plays a role in the RO frequency but is independent from *NFS*.

$$NFS = \frac{\Delta f_{RO,PI}}{f_{RO}} = \frac{f_{RO,PI}}{f_{RO}} - 1 \tag{7}$$

$$NFS = \int_0^1 \frac{\tau_0 d\rho}{\tau(V_{DD}(\rho))} - 1 \tag{8}$$

An asymmetric structure of the interference waveform may arise, as shown in Fig. 1(a). However, some interference waveforms present symmetrical bipolar structures (refer to Fig. 1(b)–(f)). The frequency shift of RO under PI can be positive, negative or zero, depending on $\tau(V_{DD})$. If the average voltage of the interference is zero, however, the frequency shift may not be null.Negative disturbances are usually generated by the circuit itself and interfere with the oscillator. The switching activity introduces impulses and steps on the power supply, as shown in Fig. 1(g) and (f). Although the frequency shift of RO is negative, $\overline{f_{RO,PI}}$ is not necessarily at the frequency of the average V_{DD}.

The frequency shift depends on $\tau(V_{DD})$ and ρ. For PI, ρ is related to the waveforms rather than to T_{PI}, whereas $\tau(V_{DD})$ is characteristic of the inverters. Thus, interference waveforms and amplitudes result in different frequency shifts. In these cases, Eq. (8) could be considered as a function of oscillator frequency modulation.

The valid range of (8) can be expressed as (9). In the condition of (9), N_{m_sw} is the necessary number of the switched gates within one interference cycle. The other parameter, N_{m_PI}, is the necessary number of interference cycles within one RO cycle. Given an RO, the valid range of (9) is determined by these two parameters.

$$N_{m,sw}\tau_0 < T_{PI} < \frac{T_{RO}}{N_{m,PI}} \tag{9}$$

The following sections aim to verify (8) and (9) through simulations and measurements.

3. Simulations and results

Simulations were performed analyzing the time domain because of the time-varying nature of oscillators [9]. Consequently, transient analysis was considered in the response of RO to PI on the power supply for a large number of oscillation periods, with HSPICE simulation steps of 1 picoseconds. The transistors used were BSIM model from SIMC 0.35-μm and 0.13-μm CMOS process. Two ROs with parameters given in Table 1were designed as DUTs for simulations.

The base circuits we used are 1801 inverters connected in a feedback loop, sharing the same power supply and ground voltages. Each inverter consists of a NMOS and a PMOS transistor with both gates and both drains connected. The power and ground pins of inverters were supplied with a series connection of a DC source and a PI source, as shown in Fig. 2. The output of the DUT was connected to a voltage probe that monitored the output waveforms of RO.

In order to obtain the static response of inverter delay, V_{PI} was set to 0 V, the step of V_{DD} was 50 mV, and each inverter in the RO was assumed to contribute an equal gate delay. Therefore, the inverter delay can be extracted from the RO cycle time based on (1), as shown in Fig. 3.

As 0.35-μm CMOS inverters turn on at 2.0 V, the amplitude of PI voltage should be smaller than 3 V when the DC supply voltage is 5 V. Likewise, when using a fixed supply voltage of 1.2 V, as 0.13-μm CMOS inverters turn on at 0.54 V, the amplitude of PI voltage should be smaller than 0.66 V. Thus, the amplitude of the interference was swept from 0% to 50% of V_0 while f_{PI} are swept from 6 MHz to 1 GHz. In order to obtain the frequency shift, 8 types of PI were added to the power supply and the responses of RO were simulated.The probability density function of each interference waveform was obtained by a statistical analysis using MATLAB. Based on (8), the predicted normalized frequency shift can be computed. The duration of 20 cycles was measured from the simulated waveforms of RO and the averaged value of $\overline{f_{RO,PI}}$ was then obtained. The normalized frequency shifts from simulations are compared with the predicted values from (8) in Figs. 4and 5, which show a suitable matching. The fitness between simulations and predicted values is observed over a wide range of interference frequency and amplitude. Therefore, the accuracy of (8) is evident over all simulation conditions.

4. Experiments and results

In this section, the response of RO to PI on the power supply is experimentally measured. The experimental setup is given in Fig. 6. The power supply was capable of measuring the static response of the inverter delay, whereas on-board voltage regulators (VR) were used in the PI test.

Two of the same ROs were mounted on the test board, one being the