Int. J. Electron. Commun. (AEÜ) 79 (2017) 151–157

Contents lists available at ScienceDirect

International Journal of Electronics and Communications (AEÜ)

journal homepage: www.elsevier.com/locate/aeue

Regular paper

Analysis of nanometer-scale InGaAs/InAs/InGaAs composite channel MOSFETs using high-K dielectrics for high speed applications

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ARTICLE INFO

Article history:
Received 7 March 2017
Accepted 4 June 2017

Keywords:
Atomic layer deposition
Composite channel
Drain-current enhancement
High-K
InAs
InGaAs MOSFETs
InP
Leakage

ABSTRACT

The outstanding electron transport properties of InGaAs and InAs semiconductor materials, makes them attractive candidates for future nano-scale CMOS. In this paper, the ON state and OFF state performance of 30 nm gate length InGaAs/InAs/InGaAs buried composite channel MOSFETs using various high-K dielectric materials is analyzed using Synopsys TCAD tool. The device features a composite channel to enhance the mobility, an InP spacer layer to minimize the defect density and a heavily doped multilayer cap. The simulation results show that MOSFETs with Al_2O_3/ZrO_2 bilayer gate oxide exhibits higher gm/I_D ratio and lower sub threshold swing than with the other dielectric materials. The measured values of threshold voltage (V_T), on resistance (R_{ON}) and DIBL for Lg = 30 nm $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ composite channel MOSFET having Al_2O_3/ZrO_2 (EOT = 1.2 nm) bilayer dielectric as gate oxide are 0.17 V, 290 Ω-μm, and 65 mV/V respectively. The device displays a transconductance of 2 mS/μm.

1. Introduction

In recent years, there have been considerable interest in the development of InGaAs or InAs channel based MOSFETs. Various research groups have proposed different device architectures using InGaAs or InAs channel based on advanced techniques such as material engineering, source \ drain (S/D) engineering and gate engineering [1–5]. The reason for considering InGaAs or InAs as channel material is that these materials exhibit very high electron mobility, higher electron velocity saturation, good thermal conductivity moreover their low voltage operation compared to silicon, SiGe, and GaAs, semiconductor technologies. There is a huge demand for Integrated circuits (ICs) based on low voltage, high speed InGaAs or InAs channel based III-V MOSFETs since these devices are widely used in applications like video conferencing, real time multimedia file transfer, high data rate internet, and also in the RF front-ends of smart mobile phones. Also ICs based on InGaAs or InAs materials are intensively studied for new millimeter and THz applications like Wireless LANs, high speed fiber-optic links, and many defense and space communication systems. InGaAs MOSFETs based integrated circuits are also under intense research for new milli-meter wave applications such as collision avoidance radars, satellite communications and giga-bit wireless LANs.

InGaAs channel based high quality metal oxide semiconductor structures with high-K dielectric materials as gate oxides are attractive candidates to become the first true THz electronics technology. Complementary metal-oxide-semiconductor (CMOS) devices based on silicon material have been scaled for more than five decades in order to achieve higher packing density, lower voltage operation, high speed and lower power consumption. As silicon CMOS device scaling is reaching its physical and optimal limits, the scaling of CMOS devices in the future in accordance with Moore's law and to meet the demands of ITRS (International technology roadmap for semiconductors) roadmap will require innovative device architectures as well as alternate materials for gate dielectrics and channels [1–4]. In the past, due to the lack of high quality thermodynamically stable oxides, the researchers were not able to reap the full benefits of the excellent electron transport properties of the III-V compound semiconductors for III-V MOSFETs [5]. The off current (I_{off}) and supply voltage (V_{DD}) are the two most significant factors which determine power consumption of MOSFETs. Gate leakage (I_G), gate induced drain leakage (GIDL) and subthreshold leakage are the main factors contribute to the off current. Hence in order to construct a MOSFET with high switching speed, high drive current and lower power consumption, it is required to minimize the off current and supply voltage. Employing high-k dielectrics such as Al_2O_3, HfO_2, ZrO_2 or TiO_2 can significantly improve the device performance. The properties of these high-K dielectric materials are given in Table 1.

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http://dx.doi.org/10.1016/j.aeue.2017.06.004
1434-8411/

Table 1
Properties of High-K Materials [1,50–52,59].

Properties	SiO_2	Al_2O_3	HfO_2	ZrO_2	$La2o3$	TiO_2
Dielectric constant	3.9	8–9	18–25	18–30	20–36	40
Band gap (eV)	9	8.8	6	5.8	4.3	3.5
Band offset for electrons (eV)	3.5	2.8	1.5	1.4	2.3	1.2
Band offset for holes (eV)	4.4	4.9	3.4	3.3	0.9	1.8

2. High-K dielectrics for next generation MOSFETs

Scaling of MOSFETs has been the basis for the semiconductor and computing industries for nearly 50 years. Traditional silicon CMOS devices with SiO_2 as gate oxide have been pushed to their limits, and therefore new materials such as high-K gate dielectrics and metal gate electrodes and new device structures are required for the continuation of Moore's law over the next 10 years [6,7]. Recently, InGaAs material has emerged as the most attractive non-silicon channel material for future nano-scale CMOS. Integration of high-K dielectrics with InGaAs channel improves the speed and enhances the scalability [7–21]. The popularity of InGaAs channel is mainly due to two reasons. First reason is the outstanding mobility of electrons in InGaAs channel as the InAs composition increases from 0 to 100%. Second reason is the rapid developments in the fabrication techniques such as atomic layer deposition (ALD) for the deposition of high-K dielectrics. The main requirement for InGaAs MOSFETs is a high quality gate oxide-semiconductor interface which can be achieved by using ALD. Many researchers have demonstrated excellent Al_2O_3/InGaAs interface for surface channel MOSFETs by ALD [22–30], which is insufficient for the next generation nano-scale MOSFETs.

In recent years, there were many reports on inversion-mode surface channel InGaAs MOSFETs realized using atomic layer deposition [22–29] technique which uses Al_2O_3, HfO_2, ZrO_2, La_2O_3 or HfAlO as gate dielectric materials and Si, Ge, Si_xN_y, Ge_xN_y, or Al_xN_y as interfacial passivation layer (IPL) and high-κ gate stacks [30–54] which shows excellent output and transfer characteristics. However, InGaAs channel based surface channel MOSFETs suffer from mobility degradation results due to various temperature dependent scattering mechanisms like phonon scattering, Coulombic scattering and optical phonon scattering. Moreover, the surface channel MOSFETs exhibits higher gate leakage current compared to buried channel InGaAs MOSFETs [1]. Also the surface roughness at the oxide channel interface limits the peak mobility of InGaAs surface channel MOSFETs. Interface charge trap density at the oxide-semiconductor is another big concern in surface channel MOSFETs. Therefore InGaAs or InAs channel based buried channel MOSFETs are being considered as the most attractive MOSFET technology for next generation CMOS technology for future logic applications. Buried channel MOSFETs have the advantage of high thermally stable oxide-semiconductor interface. Since the buried channel MOSFETs does not suffer from severe scattering effects, its channel mobility will be very high compared to surface channel MOSFETs. The higher mobility of electrons in the channel of buried channel MOSFETs is due to the use of thick InAlAs barrier layer which reduces the gate leakage, minimizes surface scattering and also plays a major role in confining the electrons in the channel.

3. Device structure and simulation results

In this work, an $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ quantum well (QW) layer structure was used as shown in Fig. 1. The device is designed for a gate length (L_g) of 30 nm. From top to bottom of the device, the epitaxial layer structure consists of a heavily doped 20 nm thick n-type $In_{0.7}Ga_{0.3}As/In_{0.53}Ga_{0.47}As$ multi-cap layer, 2 nm thin

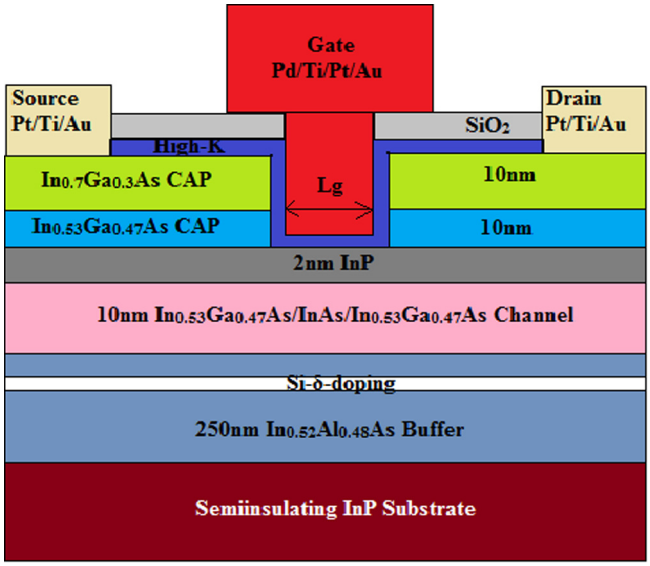

Fig. 1. Device structure of $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ Composite Channel QW-MOSFET.

InP insulator layer which reduces the access resistance and also improves the charge control, a 10 nm $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ (3 nm/4 nm/3 nm) composite channel, an inverted Si-δ-doping ($2 \times 10^{12}/cm^2$) 5 nm below the composite channel inside the $In_{0.52}Al_{0.48}As$ buffer layer and a 250 nm $In_{0.52}Al_{0.48}As$ buffer layer on top of semi insulating InP substrate. The inverted Si-δ-layer supply carriers to the S/D access regions which also reduces the S/D series resistance. The EOT used in the device design is 1.2 nm. The gate metal stack consists of Pd//Ti/Pt/Au metal layers. In this paper, the device performance for $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ composite channel MOSFETs with various gate dielectric materials such as Al_2O_3, HfO_2 and Al_2O_3(1 nm)/ZrO_2 has been studied using TCAD tool. The relationship between carrier mobility and carrier density in 30 nm gate length QW-MOSFET is shown in Fig. 2.

For EOT = 1.2 nm, an Lg = 30 nm composite channel QW-MOSFET with Al_2O_3, HfO_2 and Al_2O_3(1 nm)/ZrO_2 as gate oxides exhibits a mobility of 9600 cm^2/V-Sec, 9900 cm^2/V-Sec and 10,300 cm^2/V-Sec respectively at an inverted Si-δ doping of $2.6 \times 10^{12}/cm^2$. The mobility of electrons decreases with respect to increase in carrier density and this is mainly due to various scattering mechanisms such as coulomb scattering and phonon scattering. Phonon scattering is independent of carrier density and it is dominant at high temperatures. On the other hand coulomb scattering depends on carrier density since the carriers significantly screen the electric field of the interfacial charges and therefore change the effective potential in the composite channel. Sheet charge density in the channel increases with respect to gate voltage. If the carrier density in the channel is less than $2.6 \times 10^{12}/cm^2$ the carrier mobility increases with increases in carrier concentration in the channel and when the carrier density is higher than $2.6 \times 10^{12}/cm^2$, the mobility starts to decrease with further increase in carrier density. As the carrier density starts to saturate with increase in gate voltage, the separation between interfacial charges and the carriers decreases which leads to the decrease of the mobility due to increase in coulomb scattering.

The interfacial layer at the High-k/InGaAs channel interface is a key to reduce the border traps, interface traps, coulomb scattering from interface charge density and surface roughness scattering. A thin InP layer on top of the composite channel reduces these traps. In this work, interface trap model was included in the TCAD device