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Design of quaternary 4–2 and 5–2 compressors for nanotechnology☆

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ABSTRACT

Recently, Multiple Valued Logic (MVL) has attracted attention, because it reduces the area and complexity of circuits when compared to binary logic. Carbon nanotube field effect transistors (CNFET) are a good candidate for implementing MVL logic circuits, since determining the threshold voltage value of CNFET is easily achievable by changing the diameter of the nanotubes which are placed under the transistor gate. In this paper, quaternary CNFET based 4–2 and 5–2 compressor cells have been proposed. The proposed cell designs were investigated using HSPICE simulator with the standard 32 nm CNFET technology under different operational conditions such as different temperatures, different load capacitances, and different supply voltages. Also the sensitivity to process variations and noise immunity of the proposed designs have been investigated. The proposed quaternary logic designs reduce the delay of the multi operand addition of arithmetic circuits by eliminating the carry propagation overhead.

1. Introduction

The feature size reduction of transistors to submicron dimensions potentially results in decreased gate control, short-channel effects and high power densities [1]. In order to continue the Moore's law for reducing the size of transistors and increasing the complexity of the die area, MOSFET transistors are being investigated to be replaced with new emerging nanotechnologies. Quantum dot Cellular Automata (QCA) [2], Single Electron Transistors (SET) [3] and carbon nanotube field effect transistors (CNFET) [1] are some of the new technologies which could replace MOSFET transistors. Among these candidates, CNFET devices are more promising because of the inherent characteristics similarities between CNFET and MOSFET transistors [4]. CNFETs benefit some important features such as they have near ballistic characteristics, unique one dimensional band structure which suppress backscattering [1] and also CNFET devices have lower power consumption and higher performance in comparison to MOSFET transistors [5]. Therefore, they are appropriate for low power and high frequency applications. Another feature of CNFET devices is that if PFET and NFET transistors have the same geometries, they have the same mobility and current drive capability. This characteristic simplifies transistor sizing for complex circuits [5]. Another

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feature of CNFETs is that their threshold voltage depends on nanotube diameters and consequently in order to change transistor threshold voltage we can simply change the diameter of nanotubes which are placed under the transistor gate [6]. This feature alone makes CNFETs well suited for Multiple Valued Logic (MVL) circuits, allowing efficient way of implementing different logic levels. This important feature of them causes to use CNFETs in voltage-mode MVL logic [4].

MVL is based on using more than two logical levels for representing values. Traditional digital circuits that use binary logic have more complicated circuits than MVL logic. In recent years, MVL design has attracted more attention than binary logic. MVL logic reduces the number of operations that should take place for a specific arithmetic function and consequently they have less delay and less area for implementing the same function [7]. They can also be used for MVL logic in binary ICs to increase the circuit performance [8].

Two common designs of MVL logic are ternary and quaternary radices. Among all radices that exist for MVL logic, e (2.718) base operation has the most efficient implementation [9]. But due to the hardware restrictions for implementing real systems, one should use natural numbers as the base of computations. Also power of two radices is efficient because converting them to a binary number is simple and also they have a faithful representation for a fixed number of bits. So radix 3 which is the nearest natural number to e, and also radix 4 which has a faithful representation with the same number of bits as radix 3, are more attractive and as a result, quaternary logic leads to less complexity and production cost because of the faithful representation of the numbers in it.

Due to the important role of multiplier circuits in arithmetic operations and for reducing the number of partial products generated in multiplying operations, compressors should be used. Quaternary logic reduces the delay of addition operation because quaternary addition has no carry propagation in the critical path. In another word, if arithmetic operations are done in radix 4, five numbers in a fixed time without any carry inputs and outputs can be added. This paper presents quaternary 4–2 and 5–2 CNFET-based compressors. The proposed designs are based on converting quaternary to binary conversion and vice versa.

In the remainder of the paper, Section 2 presents carbon nanotube characteristics in details. The proposed work has been represented in the Section 3. Simulation results are demonstrated in Section 4, and finally Section 5 concludes the paper.

2. Carbon nanotube field effect transistors (CNFET)

Carbon nanotube is a sheet of graphite that is rolled as a tube. Electrical characteristics of CNTs depend on the indices of chiral vector that determine the direction of rolling sheets. The chiral vector has n1 and n2 indices. Electrical features of CNTs depend on the relation of these two chiral indices. For example if $n_1 - n_2 = 3k$ $(k \epsilon Z)$ CNT has metallic characteristics and otherwise it is a semiconductor [10].

CNTs can be Single Wall CNT (SWCNT) or Multi Wall CNT (MWCNT). The first type is made by one tube and the second type is made by multiple nanotubes that are nested inside each other [11]. SWCNTs with semiconductor electrical characteristics are used in gate channel of CNFETs [6].

Several SWCNTs could be placed next to each other under the transistor gate. The width of the transistor gate is dependent on the number of these SWCNTs and the distance between them. The distance between the centers of two adjoining tubes under the same gate of a CNFET, is called a pitch. So the width of transistor gate is determined by the following equation [12]:

$$W_{gate} \cong Max\ (W_{min},\ N \times Pitch) \tag{1}$$

where N is the number of SWCNTs which are placed under the transistor gate and W_{min} is the minimum width of the gate.

For CNFETs their threshold voltage depends on the diameter of nanotubes that are placed under the transistor gate. The following equation determines the relationship between nanotube diameters and threshold voltage of a CNFET [12]:

$$V_{th} \cong \frac{E_g}{2e} = \frac{\sqrt{3}}{3} \times \frac{aV_\pi}{eD_{CNT}} \cong \frac{0.43}{D_{CNT}\,(\mathrm{nm})} \tag{2}$$

In this case, V_π is the carbon π–π band energy in the tight bonding model, e is the unit electron charge, a is the carbon to carbon atom distance and D_{CNT} is the diameter of nanotubes which could be calculated by the following equation [12]:

$$D_{CNT} = \frac{a \times \sqrt{{n_1}^2 + {n_2}^2 + n_1 n_2}}{\pi} \cong 0.0783 \times \sqrt{{n_1}^2 + {n_2}^2 + n_1 n_2} \tag{3}$$

At the above equation, n_1 and n_2 are indices of chiral vector. So by determining these indices, threshold voltage of the CNFET is specified.

Based on the connection type between source and drain of CNFET and CNT channels, CNFETs can be considered to be one of the three types. Shottckey-Barrier (SB) types of CNFETs have a direct contact between metal and semiconductor in drain and source. This feature increases the resistance and consequently reduces the ON current capability which reduces the transistor performance. Another feature of SB transistors is that they exhibit strong ambipolar characteristics. So this type could not be used in CMOS logic families [10]. To overcome the SB problems of CNFET, second type of circuit has been introduced which behaves like MOSFET transistors. Drain and source of this type of CNFETs has been doped and they have field-effect and unipolar characteristics. Because of the lack of SB effect in MOSFET-like CNFETs, OFF current leakage