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# 3D network-on-chip design for embedded ubiquitous computing systems

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ABSTRACT

Ubiquitous High-Performance Computing applications, such as cyber-physical systems, sensor networks and virtual reality require the support of terascale embedded systems that can deliver higher performance than current systems. Multi-cores, many-cores and heterogeneous processors are becoming the typical design choices to satisfy these requirements. Inter core communication has been one of the major challenges as it affects the bandwidth and power consumption of the multi-cores processors. Network-on-Chips (NoCs) present a fast and scalable interconnection solution to fulfill the requirements of Ubiquitous High-Performance Computing applications. This paper proposes a novel 3D Network-on-Chip called Octagon for Ubiquitous Computing (OUC) that is designed for Embedded Ubiquitous Computing Systems. OUC provides low network diameter and path diversity. Simulation results show that the proposed topology achieves a significant decrease in latency and an average 21.54% and 12.89% improvement in average throughput under hotspot and uniform traffic pattern respectively.



## 1. Introduction

Ubiquitous computing is a novel concept that constructs an environment with full of computing and communication ability, and the users could not feel the presence of the computers, sensors and other machines with UC. The communication with these machines must be performed in a transparent way. Ubiquitous computing can remove the constraints of time, space and media for users to access the computing resources [1]. With the development of embedded ubiquitous computing, terascale embedded System-on-Chip (SoC) [2] with many-cores processor support becomes an urgent requirement. Motived by the rapid development of semiconductor industry, hundreds and even thousands of cores are integrated in one single chip [3–5]. The interconnection between cores in SoC has become a critical problem that must be taken into account in high performance many-core processor design [7].

To achieve efficient interconnection among cores, many on-chip interconnection communication structure were proposed. The shared bus is a traditional interconnection structure for SoC, but it suffers a lot from its limitations in bandwidth, power consumption and clock synchronization. The bus interconnection lacks scalability as the routing complexity increases dramatically with the growth of the number of cores. Network-on-Chip (NoC) has been proposed as a novel interconnection approach to overcome the limitation of traditional buses for chip design [6,7,13]. NoC takes the concept of computer networks into SoC design to separate the processing units and communication units. NoC has a better scalability, power consumption and it solves the problem of clock synchronization. Fig. 1 shows a typical NoC with $3 \times 3$ 2D-Mesh topology. A NoC-based system consists of processor elements (PE) and a communication network in any topology, such as mesh, torus ring, and etc. [15]. The PE connects the communication network using Network Interfaces (NI), and links in NoC connect routers and NI or other routers. The PE can be any implementation of processor such as DSP, memory, and any other embedded modules [14]. NoCs have caught many companies' and researchers' attention. For example, Intel has developed an 80-core Teraflop Research Chip [16] and a 48-core Single-chip Cloud Computer [17] using 2D-mesh NoC in 2007 and 2009 respectively. In 2013, MIT's $EM^2$ [18] processor integrated 110 cores in a single die using 2D-mesh NoC interconnection. All of these processors have gained large bandwidth and lower power consumption by using NoC.

Topology is a key factor in NoC research since it concerns the layout and connection of nodes and links. Topologies with different

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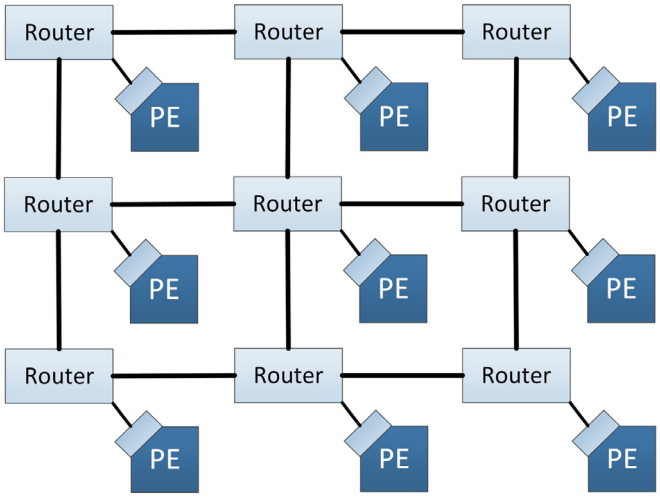


**Fig. 1.** A typical mesh-based NoC.

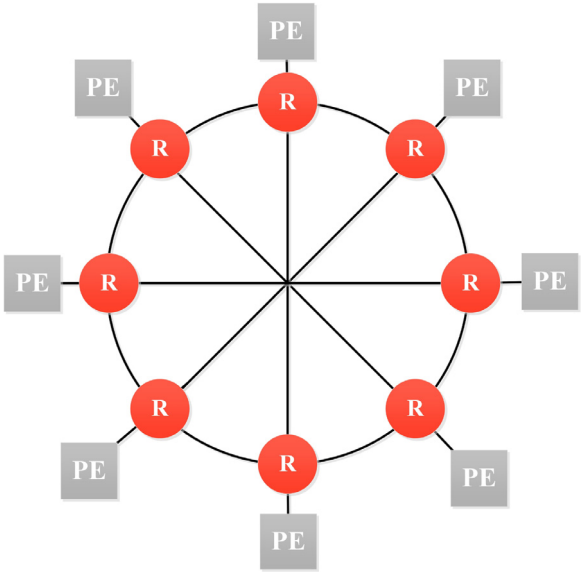


**Fig. 2.** Octagon topology.

scales and layouts should be designed to satisfy the requirements of different computing systems. Beside of the network dimension, diameter, average distance and bisection bandwidth, many other factors such as throughput, latency and power consumption should also be taken into account in the evaluation. Many topologies including 2D-mesh, 2D-torus [7], Octagon, Cluster Mesh, TinyNoC [9], DCell [11], Twisted Cube [10,12] and Honeycomb Mesh [8] have been proposed and analyzed since the birth of NoC. Fig. 2 shows Octagon [25] that was proposed by F. Karim et al. It was used to solve the problem of lacking scalability for buses in SoC. Each of the router nodes has 3 neighbor nodes. This architecture provides short average distance, since the distance between any pair of nodes is 2 hops. But the router that connects two Octagons can be a bottleneck of communication with the increase of the number of the nodes. M. Saneei et al. proposed Cluster Mesh (CMesh) [26], where each router in the network connects more than one cores. As Fig. 3 shows, every four cores are connected to one router, and this structure forms a cluster in CMesh. The average distance between each pair of cores is reduced. But cluster-based topologies need the support of routers with more ports, which increases the complexity and area of the network.

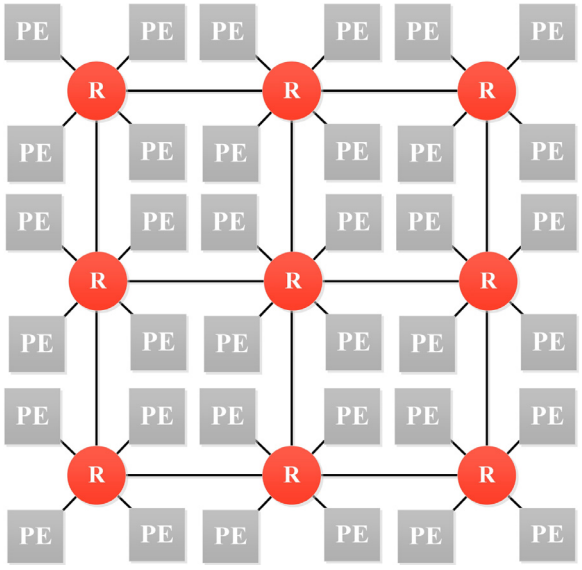


**Fig. 3.** Cluster mesh topology.

With the increase number of the nodes in NoC, traditional 2D architectures suffer a severe limitation of chip area. The development of integrated circuit technology contributes to the 3D topology design for NoCs, which becomes a trend of future NoC design due to the less chip area and shorter links [19,20]. Through Silicon Via (TSV) is a newly introduced technology for 3D NoC design [21] which increases bandwidth between layers and reduces the chip area and communication latency. Since TSV reduces the length of vertical links between layers to $\mu$m level, the latency for a packet transmitted through vertical links is largely reduced. Many techniques such as 3D DRAM stacking [22] and Solid-State Drives [23] are using 3D TSV technology.

To overcome the disadvantage of latency and area of 2D NoC, we proposed a novel 3D NoC topology OUC for embedded ubiquitous computing in this paper. This topology provides a low network diameter and path diversity to ensure low network latency and network balance. We also propose a minimal routing algorithm with fine path diversity for OUC. This algorithm makes full use of all possible minimal paths to transmit the packets, which balances the traffic load to all the network and relieve congestions. Out experimental results show that the proposed topology OUC outperforms traditional 2D-mesh in latency, throughput and energy consumption. OUC achieves a significant decrease in latency and an average 21.54% and 12.89% improvement in average throughput under hotspot and uniform traffic pattern respectively.

The main contributions of our work include: (a) a novel 3D NoC topology for embedded ubiquitous computing; (b) a minimal routing algorithm with path diversity in the 3D NoC Topology; and (c) a power efficient architecture design for NoC-based embedded ubiquitous computing.

This paper is organized as follows. Section II defines the proposed 3D NoC topology OUC for ubiquitous computing systems. Section III describes the routing algorithm that is designed for OUC. The experiments and results of the comparison between OUC and 2D-Mesh are presented in Section IV. Finally, Section V concludes this paper.

## 2. The proposed topology

The proposed OUC topology adds long link to each node to shorten the distance between any pair of nodes. Besides, the extra links also provide better path diversity that benefits traffic load

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