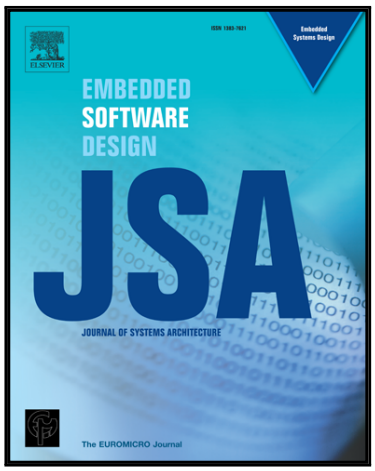

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Explore Prediction for Instruction Level Redundant Execution in Fault Tolerant Microprocessors

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Abstract

Many devices with modern microprocessor have generated an increased attention for transient soft errors. Previous strategies for instruction level temporal redundancy in super-scalar out-of-order processors have up to 45% performance degradation in certain applications compared to normal execution. The reason is that the redundant workload slows down the normal execution. Solutions are proposed to avoid certain redundant execution by reusing the result of the previously executed instructions, but there are still limitations on the instruction level parallelism and the pipeline throughput. In this paper, we propose a novel technique to recover the performance gap between instruction level temporal redundancy and normal execution. We present micro-architectural extensions necessary for implementing the reliability prediction and integrating it with the issue logic of a dual instruction stream superscalar core, and conduct extensive evaluations to demonstrate how well it can solve the performance problem. Experiments show that in average it can gain back nearly 71.13% of the overall IPC loss caused by redundant execution. Generally, it exhibits much performance and power efficiency within a high transient error rate.

Keywords: Fault Tolerance; Reliability Prediction; Double Instruction Execution;

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