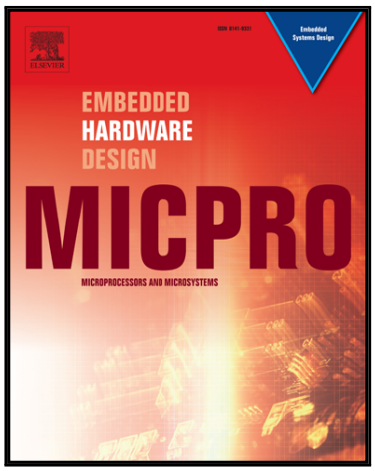

A Study on the Accuracy of Minimum Width Transistor Area in Estimating FPGA Layout Area

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A Study on the Accuracy of Minimum Width Transistor Area in Estimating FPGA Layout Area

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***Abstract*— Integrating reconfigurable fabrics in SOCs requires an accurate estimation of the layout area of the reconfigurable fabrics in order to properly optimize the architectural-level design of the fabrics and accommodate early floor-planning. This work examines the accuracy of using minimum width transistor area, a widely-used area model in many previous FPGA architectural studies, in accurately predicting layout area. In particular, the layout areas of LUT multiplexers are used as a case study. We found that compared to the minimum width transistor area, the traditional metal area based stick diagrams can provide much more accurate layout area estimations. In particular, minimum width transistor area can underestimate the layout area of LUT multiplexers by as much as a factor of 2-3 while stick diagrams can achieve over 90 percent accuracy in layout area estimation while remaining IC-process independent.**

Keywords-Field-Programmable Gate Array (FPGA); Layout; Area Estimation; Area Modeling; Silicon-On-Chip (SOC); Reconfigurable Fabric.

1. INTRODUCTION

Minimum Width Transistor Area has been used in many FPGA architectural studies [1] in estimating the implementation area of proposed FPGA architectures. The model assumes a set of basic building blocks for FPGAs and takes in a set of FPGA architectural parameters as input [1]. It then estimates the total active area that is required to implement a given FPGA architecture by counting transistors. The count assumes only minimum channel length transistors and each minimum width transistor is counted as one unit of area while the area of larger transistors are scaled as a function of their width. The approach has been considered to be a high fidelity model in ranking the implementation area of FPGA architectures [1]. Its accuracy in predicting the actual implementation area of FPGAs, however, has never been fully investigated previously.

With ever-increasing logic capacity, there are an increasing number of FPGA-based SOC designs [17][18]. These designs contain a mix of reconfigurable fabric and fixed logic in order to maximize performance and minimize power consumption of their target applications. Currently these FPGA-based SOC designs are mainly from traditional FPGA companies, which have the knowhow of designing efficient reconfigurable fabrics. Consequently these products are typically general-purpose in nature and are architected to target a variety of applications. But as architectural-level research progresses, there is increasing evidence that reconfigurable fabrics can benefit a variety of applications from processors to signal processing ASICs. Consequently there is an increasing demand for non-FPGA companies such as CPU and ASIC manufacturers to include reconfigurable fabrics on their traditionally fixed logic products. To design an efficient SOC-specific reconfigurable architecture, one must be able to accurately estimate the silicon area cost of reconfigurable fabrics as compared to other design options at the architectural design stage and be able to sweep through the various architectural parameters of a reconfigurable fabric design in order to choose the most efficient architectural parameter settings for the fabric. An accurate early estimation of silicon area also can benefit early floor-planning of the SOC and leads to a much smoother implementation of the entire design flow.

Since minimum width transistor area is the current de facto method of estimating the area of reconfigurable fabrics, and it can be easily calculated from a set of architectural specifications, in this work, we investigate the suitability of using minimum width transistor area to directly estimate the actual implementation area of FPGA-based reconfigurable fabrics. The minimum width transistor area model is first used in [3] to investigate the effect of logic cluster inputs to the implementation area of logic clusters. Subsequently, the model is used in several major FPGA architectural studies on FPGA routing area [5][19], logic cluster topology [2][6][7], effect of multi-bit routing resources on FPGA logic and routing area [8]. It also serves one of the fundamental models used by the VPR tools [1]. While the model is empirically known to have good fidelity in ranking architectural implementation areas across a wide range of FPGA designs, few studies, however, have been conducted on its accuracy corresponds to the actual layout area of these architectures.