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A blocking optimization method by convergence of cores for application-based optical circuit switched network-on-chip

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ABSTRACT

With the development of technology of integrated circuit (IC), there will be several hundred million or even several billion transistors in one chip. Optical network on chip (ONoC) has been identified as an effective communication architecture to achieve better performance in delay and energy consumption. However, in circuit switched ONoC, the blocking situation degrades the performance severely. In this paper, a method that converge intellectual property (IP) cores with the same destination address or the same source address is proposed to reduce the blocking probability in circuit switched ONoC. We compare the proposed converged circuit switched ONoC with non-converged circuit switched ONoC in terms of end-to-end (ETE) delay and energy dissipation under various applications. The simulation results show that the converged ONoC improves the ETE delay with small change in energy efficiency.

1. Introduction

With the rapid development of integration density of integrated circuit in past decades, a large number of processing elements can be fabricated in a single chip, which consist a collaborative work system to implement a specific application. It can be foreseen that there will be even more IP cores in a chip in future, however, the traditional on-chip communication based on bus will decrease the performance of chip. It is intensively studied on the electronic interconnects problems using network on chip (NoC) architecture which has the characteristics of regularity and easily to floorplan. Recent years, it is realized that many optical devices which are compatible with silicon technology could be fabricated on the chip [1–3]. And the nanophotonic waveguides can afford prominent advantage on power dissipation, latency and bandwidth compared with traditional electronic interconnects. Optical NoC (ONoC) communication architecture is proposed to take advantage of optical communication and NoC, and becomes one of the focuses of current research [4–8].

Many optical NoC architectures have been proposed that provide low power consumption and low delay communication for IP cores on system on chip [9–13]. The routing strategy they use can be classified into “active routing” and “passive routing”. The “passive routing” approach routes optical data by some fixed-wavelength [13,14], in this way, the optical data transmission can be contention-free, however, the architecture need to allocate different wavelength for different communication nodes, therefore, it is required that large arrays of fixed-wavelength light sources as well as more optical microring resonators with different resonance frequency should be integrated in this type of architecture, which costs much more area overheads and puts forward higher demand for silicon-based optical technology. In addition, the number of required wavelengths increases as more IP cores are included in one chip, but the optical wavelengths available are limited resources, so the network size hardly expands extremely [6]. Compared with “passive routing” mechanism, the “active routing” can transfer data even if only one wavelength is available, so it is easier to implement under the current technology and has the characteristic of high scalability. Because of the lack of optical random access memory, optical circuit switching is adopted in most of “active routing” achievements rather than optical packet switching which is used usually in electrical network. Optical circuit switching method sets up an exclusive data channel between two IP cores, by means of configuring the corresponding optical routers which are constituted by microring resonators [10]. Under this mechanism, data transmission blocking situation might occurs in one optical router. Although some low blocking optical routers have been proposed in [15], it is unavoidable that optical data packets come from different IP cores will compete when they go through the same out port of the route, which leads to the increase of communication delay and power consumption [16]. Because optical signals propagate at the speed of light, the delay is almost independent of the transmission

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hops [6]. The blocking situations increase the setup time of data link, and bring out great deterioration of network performance. For power consumption, the primary overheads are derived from photoelectric conversion and the electronic control network [17], however, the latter is seriously influenced by blocking on the router. If the blocking problem is not solved well, it will bring about a waste of bandwidth and energy consumption. Hence, reducing blocking probability should be an important research issue in the design flow of circuit switched optical NoC [16,18–20].

For a fixed-scale circuit switched optical network, there are limited communication resources such as links and optical routers, and the more communication nodes in the network, the more communication resources are occupied, meanwhile, the greater blocking probability occurs. Although it is viable to expand available communication resources to decrease the probability of blocking [10,21], however, these methods are all at the expense of increasing cost. As regard to the design of optical NoC for specific application, the IP cores communication graph is known, and it might be found that some IP cores sent data to one same IP core or one IP core sent data to different IP cores, in other words, some of data packets have the same source address and some have the same destination address. Learning from the optical burst switching (OBS) method [22], data packets with the same source address or destination address could be assembled into one packet, which is equivalent to reducing the communication nodes in the network, thereby, the occurrence of congestion could be decreased.

In this paper, we propose an optimization method by IP cores convergence for circuit switched optical NoC to decrease packet blocking probability. By this method, some IP cores are gathered together using grouping algorithm, so that they could be connected to the same router in network. The paper uses the method of assembling packet to reduce communication nodes in network, which decreases the blocking probability to a certain extent. The principle of this method draws lessons from optical burst switching (OBS), which has been extensively studied in macro optical communication network but rarely researched in optical NoC. The optimization method for optical NoC design is not a straightforward implementation of OBS. There is a big difference between data characteristics of the macro network and that of the on chip network for specific applications. In macro network, the burst data packets account for a large proportion of all data packets, and there is no strong correlation between the resource nodes in network, the data communication paths change dynamically. So the convergence routers in OBS network are designed to be universal, the important issues that should be discussed are data scheduling algorithm, assembly algorithm and quality of service (QoS) mechanism, and there is no need to converge resource nodes into one fixed group. But in an optical NoC which is customized for a specific application, the IP cores and their communication requirements are determined, and convergence of IP cores will improve the blocking situation, therefore grouping method should be given in detail. In addition, area and power consumption are important constraints that should be taken into account in chip design flow, so the convergence router architecture should be custom-designed. The contributions of the paper are the following: 1.The effectiveness and feasibility of assembling packets to reduce blocking have been verified by simulation. 2. A convergence router architecture for the method is proposed, and the operational principle of the router is described in detail. 3. An IP cores grouping algorithm is given. The experimental results show that the communication delays under different applications are decreased for optical NoC using the design method proposed in this paper.

The rest of the paper is organized as follows. Section 2 gives a summary of related work on optical NoC. In Section 3, the situation of blocking is analyzed in detail. Section 4 describes the optimization IP cores convergence method and a convergence optical router is proposed. Section 5 shows the experimental results, and Section 6 concludes the paper.

2. Related works

Many optical network on chip architectures based on the nanophotonic devices have been proposed in the last few years. Assaf Shacham et al. [10] presented a photonic circuit switched NoC as a solution for high-performance multiprocessors communication. The paper also proposed an extensible network structure to increase path multiplicity by using a folded-torus topology. As path multiplicity grows, the blockings in the network will be reduced, and the corresponding energy overhead consumed by setup massages is decreased. But this structure requires more router and link resources, which results in the increase of power consumption and area. Hui Li et al. [21] proposed a hybrid packet-circuit switched router for optical NoC which could support optical circuit switching and optical packet switching at the same time. This router processes the traffic of different services by assigning different wavelengths to the two types of services. This method could satisfy the requirements of two categories of traffic: the guaranteed service and the best-effort service. A WDM multi-waveguide optical NoC architecture (WWONoC) was proposed in [14]. The WWONoC utilizes the WDM technique to reduce the blocking probability. For 64 cores multiprocessors, there are eight waveguides in vertical direction, and the architecture uses eight wavelengths to realize on-chip communication. Zhang et al. [23] proposed three packet switching optical NoC architectures, it adopted WDM technique and integrated lots of buffers in the optical router. Edoardo et al. [6] proposed an algorithm which maps the IP cores onto a mesh-based optical NoC for specific applications to minimize the worst-case power loss. But the blocking problem was not solved by the algorithm. Hajar et al. [24] proposed an optical reconfigurable flat and tree NoC which could customize the topology and routing paths based on the application characteristic.

In [25], Cui-Ting Li et al. proposed a method of constructing a universal structure of N-stage cascaded 8 port optical router. In [26–28], five-port optical routers of different architectures based on microring switch were presented, and the routers could suit for the mesh-based optical NoC. In [29], a methodology that could interconnect a large number of IP cores using optical networks was proposed. The optimization for asymmetric power losses of microring resonators was investigated in the design of multistage interconnection networks in [30]. An architecture called Flyover was proposed in [31], which combines the TDM and WDM technologies to solve the congestion problem in optical circuit switching. In [32], a bufferless photonic clos network (BLOCON) and a scheduling algorithm were proposed to solve the output contention problem. In [33], the thermal effects on the 3D optical NoC was investigated. The paper [34] studied crosstalk noise in microring resonators which used in high-radix and low diameter crossbar-based optical NoCs, and proposed two novel encoding mechanisms aiming to improve worst-case SNR. The research progress of the optical router would make the on-chip communication using optical network come true in future. However, in the optical circuit switched network, the optical routers proposed until now have not solved the blocking problem thoroughly due to the competitions of multiple data packets in the same out port of the router. To the best of our knowledge, few works has been reported to decrease blocking probability by designing reasonable architecture. Thus in this paper, we propose an IP cores convergence method aiming at blocking probability reduction on circuit switched optical NoC, and a convergence optical router is designed to make the method realizable.