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FPGA implementation of wavelet coherence for EEG and ERP signals

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ABSTRACT

This paper presents the design and implementation of wavelet coherence (WC) processor on low cost field-programmable gate array (FPGA). This design is adapted to estimate the wavelet coherence between two EEG signals in a minimal delay in order to support real time applications. The produced CWT coefficients were saved in static RAM chips and prepared for the WC analysis starting with the smoothing operation as an essential computation for the WC algorithm. The WC algorithm was analyzed in the means of choosing the suitable word length for the stages of the design and to simplify the employed functions in the algorithm. Several controllers that handle signal transmission among the design components were designed using hardware description language (VHDL). By using 4 parallel-processing smoothing circuits, the design is capable to calculate the coherogram between two EEG signals (1024 point each) in a total time of 128.64 ms. Image quality methods were applied for coherogram comparison between hardware and software. Hardware results were compared against the rigorous software standard WC according to the following measures; normalized mean square error (NMSE), normalized average difference (NAD) and structural content (SC) are 0.0045, 0.0485 and 0.921 respectively.

1. Introduction

Wavelet coherence (WC) has been widely used for the study of connectivity between pairs of brain channels that represent the correlation between two electroencephalogram (EEG) waveforms at localized time and frequency [1,2]. The EEGs are very weak electrical activities produced by the brain and can be measured from different sites on the scalp using metal electrodes. The maximum amplitude for the EEG signal can go up to 100 μV and their frequency components are in the range 0.5–100 Hz [3]. However, the typical frequency range of an EEG epoch is 0.5–40 Hz [4]. Real time EEG applications are highly depend on the event related potential (ERP) components superimposed on the ongoing EEG and specifically, the P300 [5–6]. The P300 is a positive peak 300–900 ms over the EEG and can occur following a stimulus presented to the participant [7–9].

An EEG epoch of 1000 ms is sufficient to occupy the ERP P300 that plays a vital role in recent EEG applications. Examples of such applications are the brain computer interface (BCI) [10] and biofeedback studies [11]. These applications require real time algorithm processing of the data measured to provide the required information within a minimal delay [12].

WC has been used to reveal brain abnormalities and malfunctions such as the diagnosis of schizophrenia [13] or the corticomuscular functionality in detecting muscle fatigue [14]. In addition, WC may be used for biofeedback studies where typically existing biofeedback measures are normally use single electrode sites [15]. However, using two electrode sites allow a measure of the linkage (such as coherence) which taps into internal communications or possibly information processing between cortical areas, reflecting more complex cognitive activity, especially attentional filtering between these sites. A single electrode site does not have access to this and it was desired to target this functionality for biofeedback change.

Previous works in the literature showed that the computation of WC depends on the off-line processing of EEG signals due to the intensive operations included in the algorithm [1,2,13]. However, real time processing of WC for EEG signals is still in demand [14]. The involvement of WC in real time EEG applications require high speed of computation due to the complexity of the mathematical functions implied in the WC algorithm required to construct the WC plane, the “coherogram” [16]. To achieve such computation speed, the Field Programmable Gate Array (FPGA) solution is utilized as proposed in this paper.

Previous work by the authors has outlined the validity of WC in the ERP gamma band for finding significant relations related to cognition [17]. The involvement of the continuous wavelet transform (CWT) in analysing the EEG using FPGA and the effect of the

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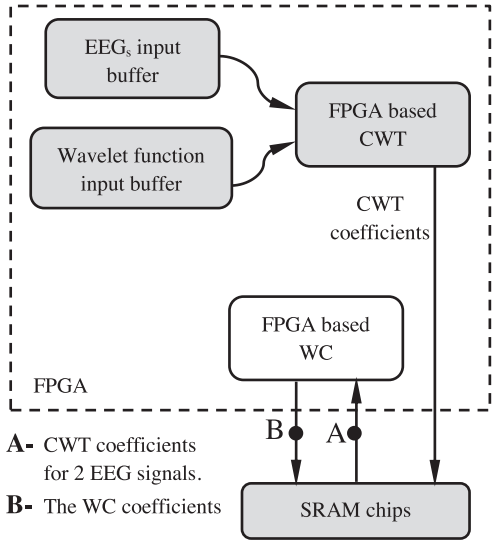

Fig. 1. The CWT design and the WC design in the FPGA with the SRAM chips used for storing results. Gray cells refer to previously developed and used blocks [20].

quantization error on the produced CWT scalogram in this design with design optimizations were previously investigated by the authors [18–20], in which the grey blocks in Fig. 1 refer. In [20] the Morlet CWT for EEG signals was implemented in the frequency domain using Spartan 3AN FPGA. The calculation of the wavelet coefficients at 37 scales was then optimized to 21 scales that are sufficient to cover the frequency range of the EEG (0.5–60 Hz). The produced CWT coefficients were stored in two SRAM chips on the FPGA platform. This paper proposes a VHDL and schematic based FPGA design implementation of the WC applied to EEG and ERP signals based on the CWT design in [19,20]. The focus is to speed up the processing of the WC algorithm thereby meeting real time requirements. The design presented in this paper is able to perform the task of WC in few milliseconds which is sensible for real time EEG applications. There is a little in the literature on the reconfigurable computing of the CWT [21–23]. However, to the best of the authors' knowledge, no previous work is found in the literature targeting VLSI mapping of WC.

The WC plane requires two wavelet planes to be constructed in addition to other involved computations including complex multiplications, smoothing, division and the Cartesian to polar conversion [1,16]. To calculate the square wavelet coherence (WC) R_n^2 between two equal length time series x and y, the following formula can be applied [16]:

$$R_n^2(s) = \frac{\left|S(s^{-1}W_n^{xy}(s))\right|^2}{S(s^{-1}|W_n^x(s)|^2 . \left(s^{-1}\left|W_n^y(s)\right|^2\right)} \quad (1)$$

where s is the wavelet scale, s^{-1} is for energy density, W_n^{xy} is the wavelet cross spectrum between x and y and W_n^x is the CWT for signal x. S is the smoothing operator in scale or time such that $S(W) = S_{scale}(W_n(s))$ or $S(W) = S_{time}(W_n(s))$.

According to the Schwarz inequality, the WC takes its values between 0 and 1. Without smoothing all the WC coefficients are trivially equal to 1. As a priority of operations, it can be noticed from (1), the numerator, that the smoothing operation S is applied before determining the absolute value and the square operation to the WCS whereas smoothing follows up the absolute value and the square operation to both auto-spectrums in the denominator. Only the magnitude WC is used in this article as it is the commonly used in analysis [2,13], and no citation to the wavelet phase coherence is included.

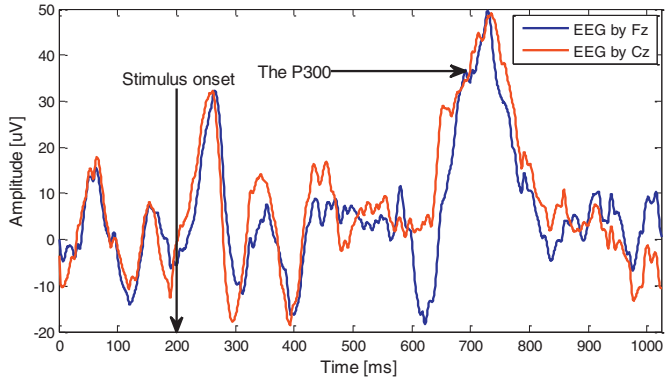

Fig. 2. Pair of simultaneous EEG epochs measured through the oddball test from the brain sites Fz-Cz and used to test the FPGA based WC design.

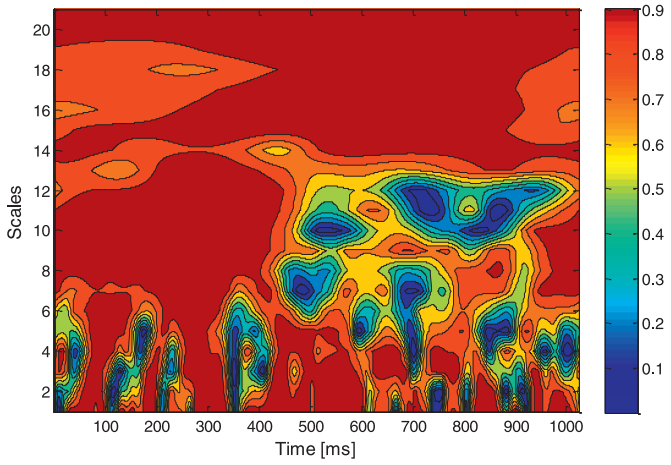

Fig. 3a. Software based wavelet coherence between the EEGs in Fig. 2. used for validation.

To apply (1) on a pair of EEG waveforms and to prepare for a reference WC diagram, two EEG signals were used from the frontal and central brain electrodes (Fz & Cz) as shown in Fig. 2. In this figure, the presented stimulus to the participant was at 200 ms and the P300 response can be seen at 600–800 ms. By applying (1) to compute the WC between the EEGs in Fig. 2, the resultant software-based (Matlab) WC is shown in Fig. 3a in graded colours ranging between 0 and 1; close to 1 means high correlation regions between the two EEGs whereas close to 0 refers to weak coherence between the two EEG epochs in the time-scale plane. Fig. 3a represents the reference WC diagram to the target figure generated by FPGA. This is because the FPGA based WC subject to the quantization error throughout the included mathematical functions in (1) that negatively affect the quality of the coherogram. This quality can be tested with image quality methods as objective indices to the hardware WC. Fig. 3b shows the resultant WC by taking the FPGA based two CWTs (point A in Fig. 1) and applies Eq. (1) to them using Matlab. The WC in Fig. 3b shows the degradation appears in the coherogram against the one in Fig. 3a as a result of using FPGA based CWTs. More degradation will be obviously added when (1) is completely performed in FPGA as this paper presents.

The structure of this paper is as follows: Section 2 introduces the EEG data acquired to test the design along with the analysis of WC algorithm. In addition, the smoothing function and the word length selection for the WC design are also included. In Section 3, the FPGA implementation with parallel data transfer and