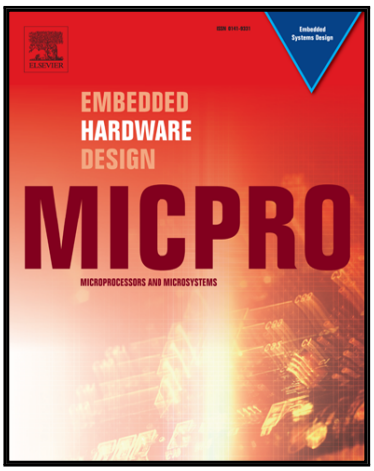

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Emulation of an ASIC Power and Temperature Monitoring System (eTPMon) for FPGA Prototyping

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Abstract

Hardware monitoring information can be used during system runtime to increase system lifetime and reliability. Examples of such monitoring information are power, temperature, and the aging status of processors. They provide the system with relevant information about the current hardware health. Such information is especially crucial in resource-aware computing concepts that introduce self-organizing behavior to deal with large MPSoCs (Multi-Processor Systems-on-Chip): For resource-aware computing, resources are allocated according to the current requirements. To find suitable resource-application pairs and achieve system targets like optimizing the utilization, current hardware status must be considered during resource allocation.

To evaluate and optimize resource allocation strategies during the design phase, FPGA prototyping is often required before its implementation in ASIC. The evolution of power, temperature and aging differ between ASIC implementation and FPGA prototype. The FPGA prototype should react on sensor data characterized from the target ASIC design instead of FPGA's hardware status.

This paper describes the design of an emulated ASIC Temperature and Power Monitoring system (eTPMon) for FPGA-based prototyping. The emulation approach for power monitors is based on an instruction-level energy model. For emulating temperature monitors, a thermal RC model is used.

eTPMon can supply MPSoC prototypes with the hardware status information (power and temperature of the cores) needed for efficient load distribution, achieving resource-aware computing targets. Based on the eTPMon data, different operating strategies and control targets were evaluated for a 2-tile resource-aware MPSoC system. Values provided by eTPMon are usable for extracting information about the aging of processors, which can be used for increasing the system lifetime.

Keywords: power monitoring, temperature monitoring, ASIC monitor emulation, monitoring systems, online monitoring

1. Introduction

With power consumption being the limiting factor for increasing integration density predicted by Moore's law [1], there is extensive research for reducing power consumption. As MPSoCs (Multi-Processor Systems-on-Chip) become more complex and include dynamic power management techniques as well as dynamic resource management techniques, the need for power monitoring has become more important for both design time (evaluation of power management and resource allocation strategies) and runtime (observing the power/energy consumption of applications for all cores).

High power densities in modern CMOS technologies affect chip temperature that also depends on the thermal conductivity of the chip and its package. Reasonably priced processor packaging, covering worst case thermal hot spot scenarios cannot be provided anymore, since as power increases, there is a non-linear relationship between the cooling capabilities of the package and its cost [2]. High temperature reduces circuit speed and causes degradation [3]. Temperature, as well as circuit aging, depends on the workload of the device [4]. So local thermal hot spots arise, if the workload is distributed in a non-uniform way in different circuit blocks, which is typically the case for processors [5]. This problem is even more critical in MPSoCs: Non-uniform temperature distribution happens not only within one single core, but also between different cores. And the temperature of a core depends not only on its own power density, but also on the activities and the power densities of neighboring cores. So, cores, even if of the same type, may behave very differently.

Altogether this can affect the lifetime and the reliability of a chip [3, 5], as aging effects like Negative-Bias Temperature Instability (NBTI) and Hot Carrier Injec-

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